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## CHAPTER 5 DESIGN SIMPLIFICATION AND RELIABILITY ANALYSIS METHODS

### 5.1 General

This chapter explains specific techniques, quality function deployment, parameter design, design for test, and FMEA to be used to design a semiconductor, taking specific examples.

### 5.2 Quality Function Deployment

Quality function deployment (QFD) was developed as a new product development tool that provides a means of communicating design concepts to the manufacturing line as well as a specific method for quality assurance.

Quality function deployment is a technique for the detailed deployment of job functions and operations to create quality, using a series of purposes and means. This technique produces favorable results by aiming to “establish design quality”, “reduce early quality problems”, “establish planned quality”, “communicate design concepts to manufacturing”, “compare and analyze our products and competitors’ products”, “help develop distinctive new products”, “clarify management issues in the manufacturing processes”, “disseminate quality information throughout the company”, “help collect and analyze market quality information”, and “reduce design changes”, and so on.

By using this technique, technologies to realize the designed quality can be developed and problems that can be foreseen can be solved systematically. This is a total quality deployment technique if it includes cost deployment that takes into consideration the price and required quality of competitors’ products, and solves bottlenecks for calculated component cost, and reliability deployment that combines a reliability technique such as FMEA to prevent failures at the design stage.

At this point, let us turn to the topic of quality tables, which play an important role in quality deployment. What are quality tables and how are they created? Quality chart is a systematic representation of terms used to describe quality-related features desired by customers. The chart shows correlation between these terms and product quality characteristics to aid the process of converting customer requirements into alternative characteristics to be used when designing products.

#### (1) Collection of raw data

Raw data is information (requirements in plain language) received from customers with regard to particular products. This is the starting point of quality function deployment.

#### (2) Translation to required quality

The raw data is organized into a list of required quality items. A more concise listing of quality-related terms is extracted from the raw data list, and this concise list comprises the “required quality.”

#### (3) Creation of required quality deployment chart

Required quality items are broken down into a multileveled chart that may include primary, secondary, and tertiary levels.

#### (4) Extraction of quality elements

Required quality items must be translated into technical terms in order to deploy customers’ abstract ideas about product quality as specific product quality characteristics. These quality characteristics are alternative characteristics that are used in place of the actual customer requirements as characteristics which can be measured and evaluated according to their quality elements (quality elements are the criteria used to evaluate quality). Usually, quality elements are extracted from the required quality items.

**(5) Creation of quality element deployment chart**

Next, quality elements are broken down into a multileveled chart that may include primary, secondary, and tertiary levels. The lowest-level items in the quality element deployment chart should be quality characteristics.

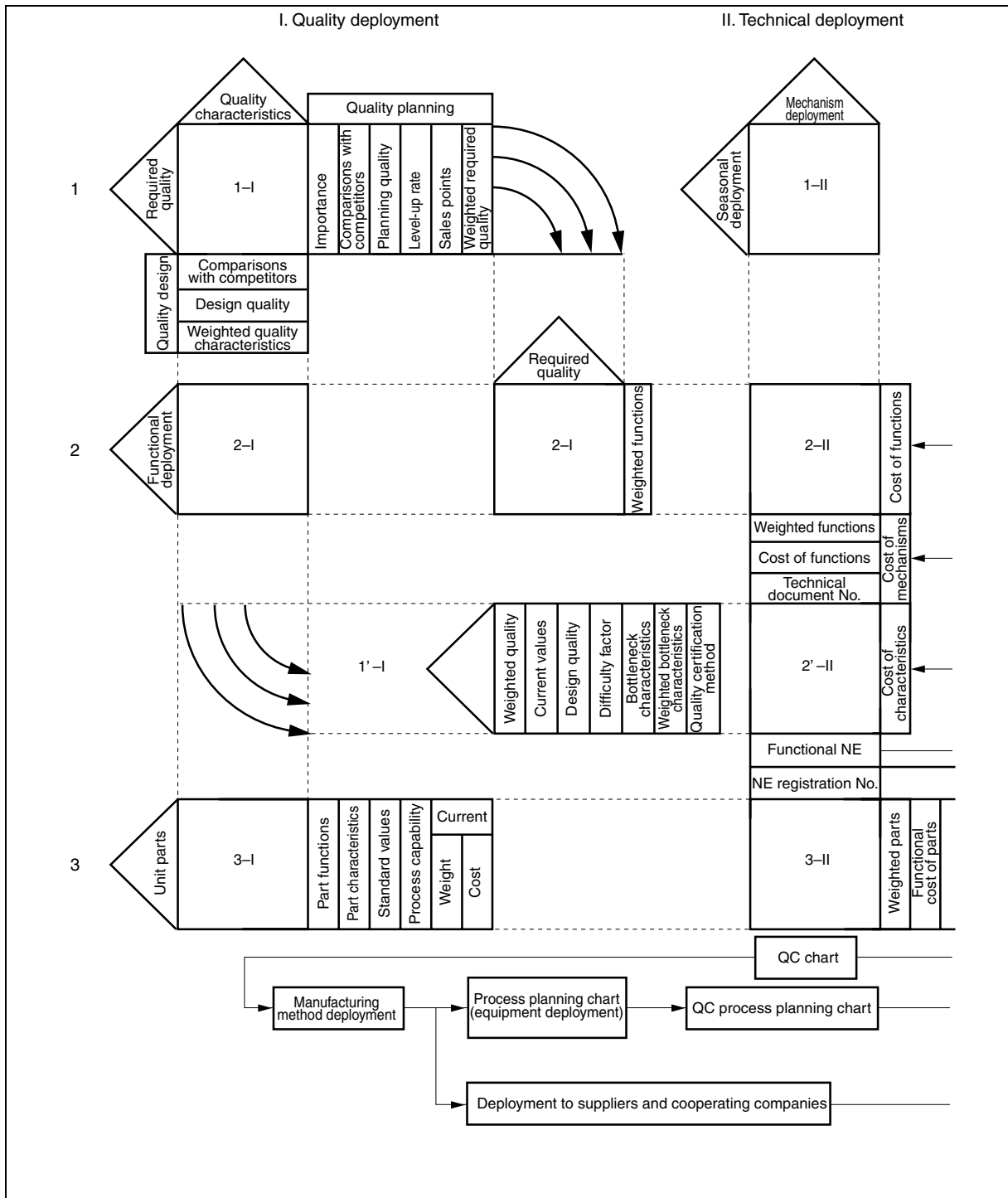
**(6) Creation of quality chart**

The required quality deployment chart and the quality element deployment chart are combined in a two-dimensional table having a matrix format.

The relative strength or weakness of the correlation between required quality items and quality elements are noted using symbols (◎, ○, △, etc.). This enables importance rankings to be assigned to the required quality items and quality elements, which helps determine which quality elements are the most important.

Figure 5-1 shows an overall outline of quality deployment and Table 5-1 shows an example of a filled-in quality chart.

Figure 5-1. Overall Outline of Quality Deployment (“House of Quality”)



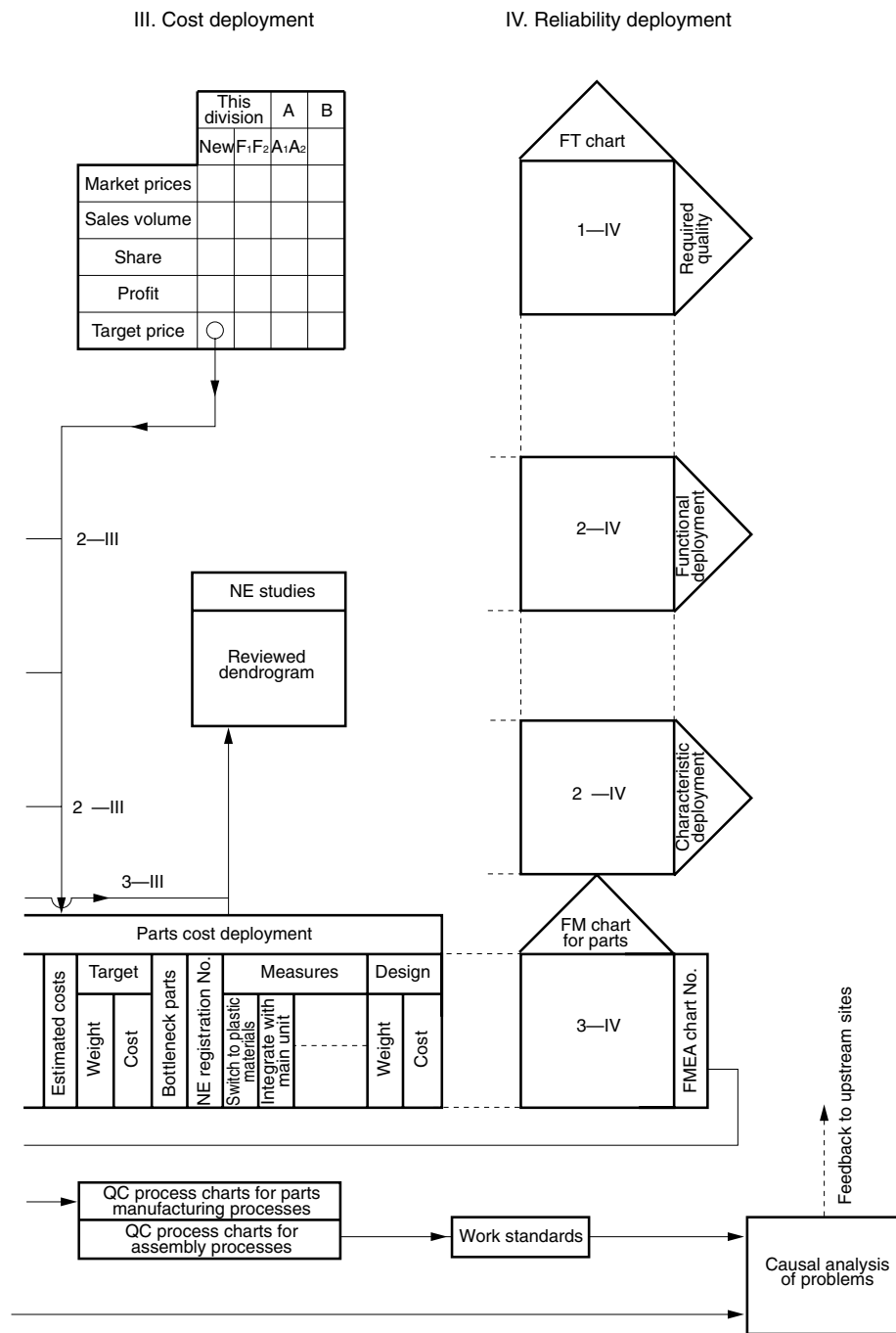


Table 5-1. Example of Filled-in Quality Chart

Quality Characteristics		Primary	Electrical Performance				Mechanical Performance		Operability			Designability	
		Secondary	TRS characteristics	R characteristics	T characteristics	S characteristics	Mechanical precision	Durability	Portability	Stability	Operability	Color scheme	Size
Required Quality													
Primary	Secondary	Importance	C	C	B	C	A	A	B	B	A	C	C
Accurate operation	No operation errors	B	△	◎	◎								
	Superior performance	A	○	○	○	○							
	Stable performance	A	◎	◎	◎	◎	○	○					
Long useful life	Break-resistant	B	△	△	△	△	◎	◎					
	Accident-proof	C		○	◎		△	◎	△	△			
Ease of operation	Easy to operate	C			△	○			○	○	◎		
	Easy to maintain	C						△	◎	◎			
Ease of handling	Easy to replace	C				△			△				
	Easy to attach	C								○	◎		
Designability	Attractive appearance	C							○	○		◎	◎
	Good color scheme	C									◎	◎	

References

- Y. Akao "Introduction to Quality Deployment" JUSE (Japanese version only)
- T. Oofuji, M. Ono and Y. Akao "Quality Deployment Methods (1)" JUSE (Japanese version only)

### 5.3 Parameter Design

#### 5.3.1 What can parameter design accomplish?

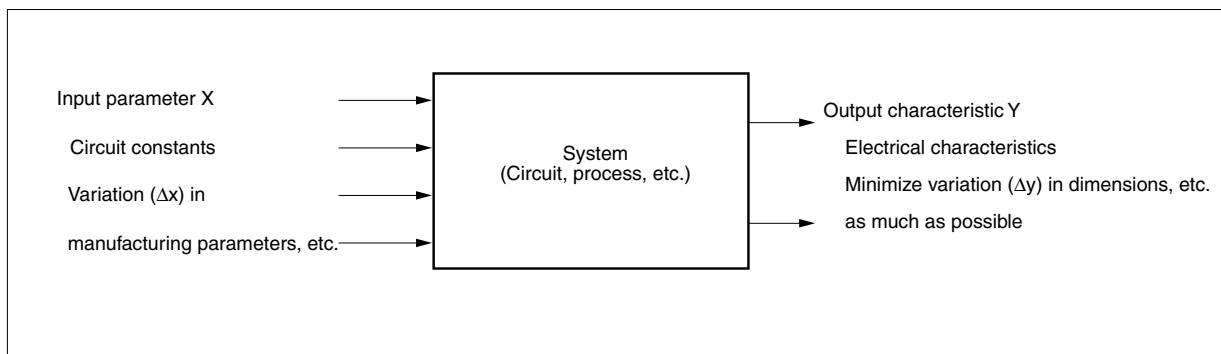
At Compound Semiconductor Devices Division, design of semiconductor products is performed based on development specifications that clearly reflect the needs of customers. At the circuit design stage, designers seek to establish a robust design that takes into account variation among manufacturing processes (a robust circuit design is a design that will not enable the circuit characteristics to be seriously affected by variation among manufacturing processes). It is also at the manufacturing design stage where variation in product dimensions, thicknesses, etc., are reduced to minimize manufacturing process variation and optimize the various manufacturing conditions and the process flow.

Thus, when circuit design, layout design, process design, device structure design, and various other aspects of design have been optimized, the result will be the building in of higher reliability.

This brings us to a definition of parameter design as design methods that minimize variation among the circuit characteristics and characteristics (parameters) that are used in manufacturing processes. The purpose of parameter design is to minimize variation among a system's output characteristics.

Generally, a large number of parameters must be established in the target system (whether it be a semiconductor device, manufacturing process, production equipment, etc.). Although a tremendous amount of tests and simulations must be performed to determine the optimum value for each parameter, parameter design offers testing and planning methods that set values for most parameters with only a minimal number of tests or simulations. The system input/output characteristics that are used in parameter design are shown in Figure 5-2.

**Figure 5-2. System's Input and Output Characteristics**



### 5.3.2 What is parameter design?

Parameter design is one of the chief methods proposed by Gen'ichi Taguchi in his book Quality Engineering. Parameter design applies to effectively optimize the numerous parameters and thus minimizes variation in the target system's output characteristics.

Four types of S-N (signal-to-noise) ratios are defined for a system's output characteristics. These four S-N ratios are used as objective functions to optimize parameters.

#### SN ratio

In the context of parameter design, the SN ratio is based on regarding the variable factors in output characteristic data as "noise" and the fixed factors as "signal". This concept of a signal-to-noise ratio is widely used in the telecommunications field, and in this case it is being extended to the field of statistical QC.

Given  $n$  as the quantity of output characteristic data:

$$y_1, y_2, \dots, y_n$$

Various statistical analyses are performed based on two statistical processes that use this "n" value:

$$\text{Average value } \bar{y} = \frac{\sum_{i=1}^n y_i}{n}$$

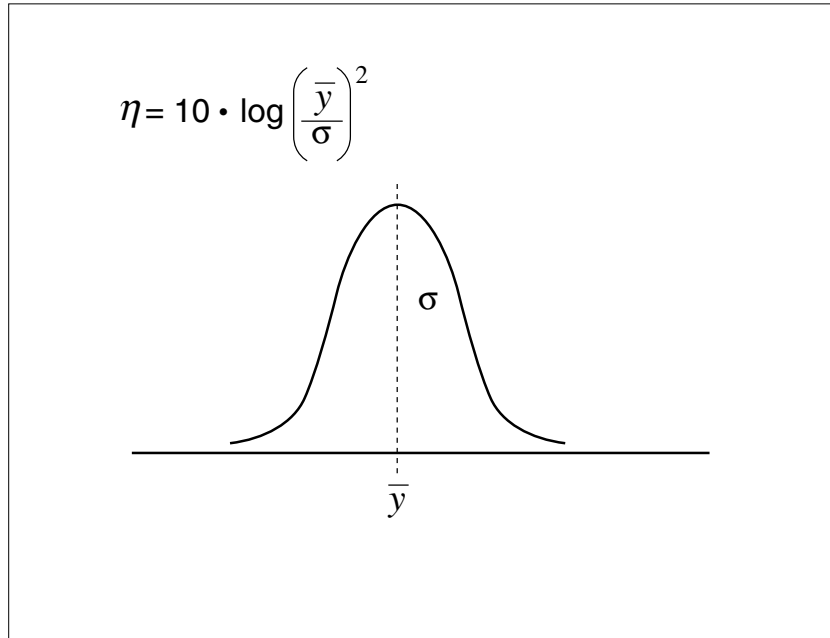
and

$$\text{Standard deviation } \sigma = \sqrt{\frac{\sum_{i=1}^n y_i^2 - n\bar{y}^2}{n-1}}$$

The four types of SN ratios are defined according to the following four types of output characteristics. The input parameters are set so as to maximize the output characteristics.

**(1) Nominal-the-better characteristics**

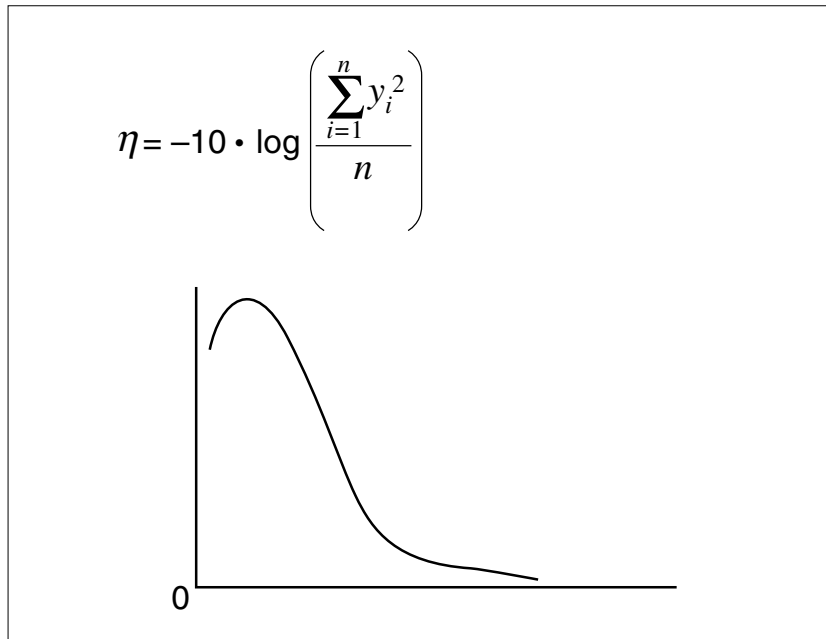
This is the SN ratio among values centered on desired dimensions, thickness, etc.

**Figure 5-3. Nominal-the-Better Characteristics Curve**

As shown in Figure 5-3, higher values on this curve result in lower variation  $\sigma$  among output characteristics.

**(2) Smaller-the-better characteristics**

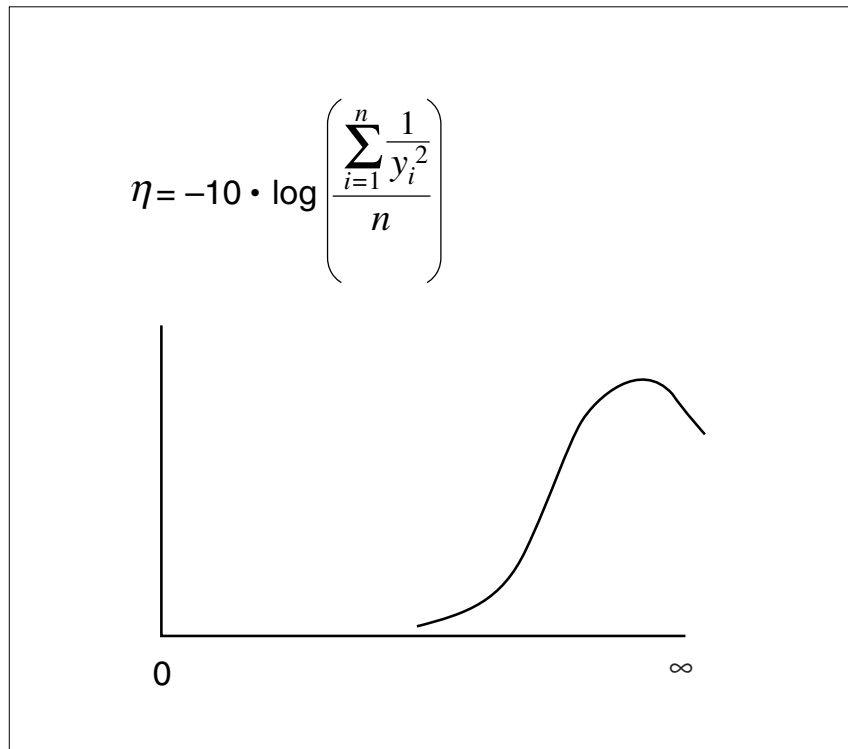
This S-N ratio applies to the desire for products free of damage or defects.

**Figure 5-4. Smaller-the-Better Characteristics Curve**

In Figure 5-4, the SN ratio increases (improves) as the total amount (sum of amount squared) decreases.

**(3) Larger-the-better characteristics**

This SN ratio improves as durability and strength characteristics increase.

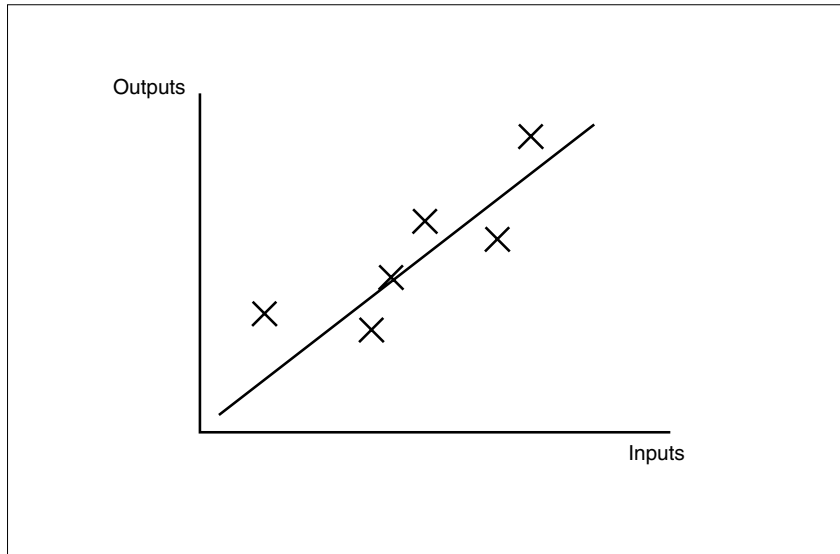
**Figure 5-5. Larger-the-Better Characteristics Curve**

In Figure 5-5, the SN ratio increases (improves) as the total amount (sum of amount squared) increases.

**(4) Dynamic characteristics**

This SN ratio applies to the required linearity, such as in the relation between mask pattern dimensions and the finished dimensions when manufactured on a wafer.

**Figure 5-6. Dynamic Characteristics Curve**



Although no formula is given to define this SN ratio, the optimum SN ratio in this case is when the values representing correlation between inputs and outputs are as close as possible to the median straight line (see **Figure 5-6**).

**5.3.3 Example of parameter design**

The following is an example of how parameter design is used as part of manufacturing process design. In device manufacturing processes, the processing of electrode wiring has a major impact on yield and reliability. The conditions for the PR and dry etching processes are especially important for the stable formation of refined wiring patterns.

The following are examples of improvements made for aluminum residues in the aluminum dry etching process. As shown in Table 5-2, eight parameters (A to H) must be established for aluminum etching processes in order to consider conditions which affect the three etching sequences, such as the presence or absence of preprocessing, four types of gas flow rates, pressure, and the bias voltage.

**Table 5-2. Aluminum Dry Etching Conditions**

	Etching Sequence		
	1st	2nd	3rd
Flow rate of gas 1	known	known	known
Flow rate of gas 2	known	known	G
Flow rate of gas 3	A	known	F
Flow rate of gas 4	B	known	known
Pressure	known	E	D
Bias voltage	known	known	C
Preprocessing	H		

The orthogonal array L18 can be used to efficiently conduct a total of 18 experiments to determine the parameters to be established as parameters A to H (see **Table 5-3**). The three number values (1 to 3) that appear in this orthogonal array indicate the level numbers of the various factors. An S-N ratio for desired characteristics is used for aluminum residues, which have a level of zero similar to dirt and defects.

Table 5-3. Orthogonal Array L18

No.	A	C	D	F	G	E	H	B	SN Ratio for Smaller-the-Better Characteristics
<1>	1	1	1	1	1	1	1	1	-5.40 db
<2>	1	1	2	2	2	2	2	2	4.77
<3>	1	1	3	3	3	3	3	3	15.00
<4>	1	2	1	1	2	2	3	3	5.74
<5>	1	2	2	2	3	3	1	1	11.76
<6>	1	2	3	3	1	1	2	2	-6.69
<7>	1	3	1	2	1	3	2	3	15.00
<8>	1	3	2	3	2	1	3	1	-6.09
<9>	1	3	3	1	3	2	1	2	1.76
<10>	2	1	1	3	3	2	2	1	15.00
<11>	2	1	2	1	1	3	3	2	15.00
<12>	2	1	3	2	2	1	1	2	3.98
<13>	2	2	1	2	3	1	3	2	-9.58
<14>	2	2	2	3	1	2	1	3	-7.27
<15>	2	2	3	1	2	3	2	1	15.00
<16>	2	3	1	3	2	3	1	2	-4.26
<17>	2	3	2	1	3	1	2	3	-5.64
<18>	2	3	3	2	1	2	3	1	-7.27

The following type of graph can be obtained by analyzing this data. (See **Figure 5-7.**)

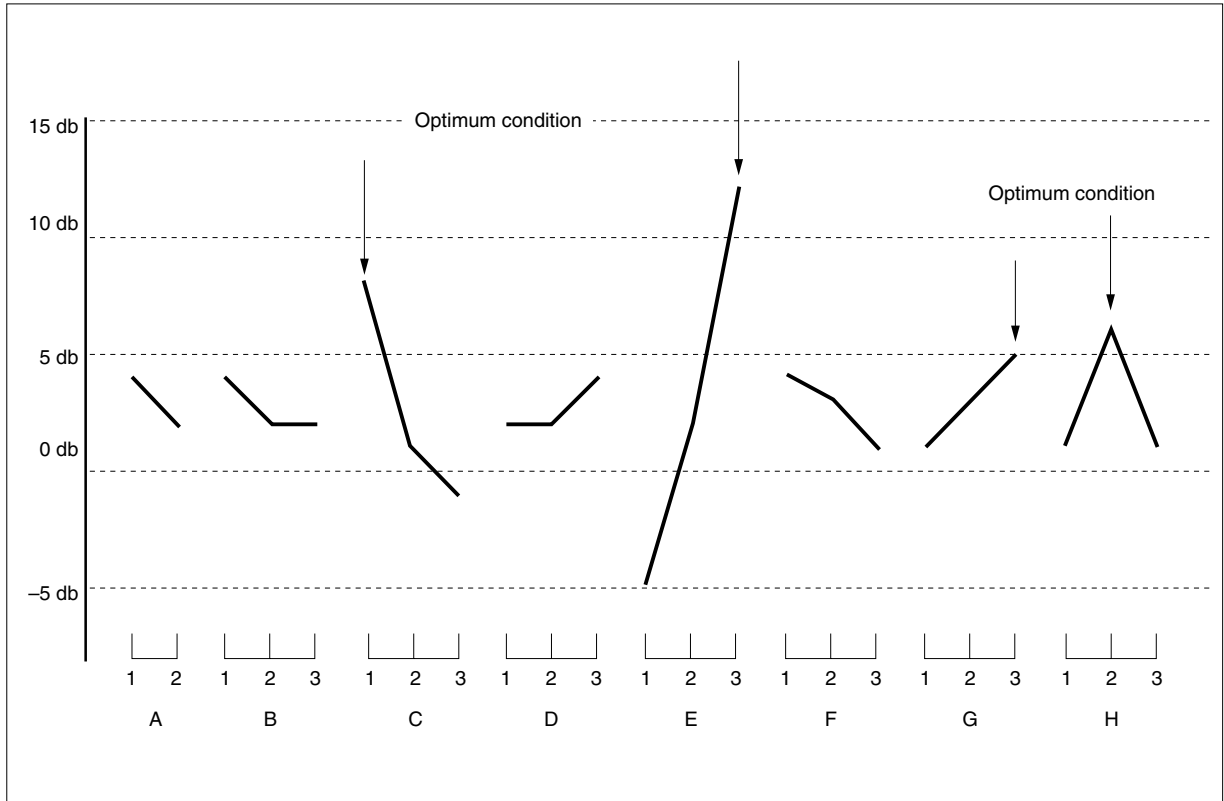
The optimum conditions for the aluminum etching processes can be determined by setting factor levels that maximize the S-N ratio indicated on the Factor Effect Graph.

In this example, four factors (E, C, H, and G) are shown to have the greatest impact on aluminum residues, and we can see that the optimal conditions in this case are E = level 3, C = level 1, G = level 3, and H = level 2.

As a result of optimizing the fabrication conditions for aluminum etching processes, the occurrence of aluminum residues can be reduced while increasing both yield and reliability.

The scope of parameter design includes not only the optimization of fabrication conditions described above but also circuit design, bias design, and other areas in which it also contributes to raising the reliability and quality of ICs.

Figure 5-7. Factor Effect Graph



**References**

- G. Taguchi "Quality Engineering Course 1: Quality Engineering at Development and Design Stages," (Japanese version only)

## 5.4 DFT (Design For Test)

The DFT (Design For Test) approach is described below as it relates to quality assurance for ICs.

The higher integration of ICs has made it more difficult to comprehensively test internal circuits. Therefore, testability must be taken into consideration beginning at the design stage.

### 5.4.1 Testability

Testability is a characteristic that indicates the relative ease or difficulty of internal testing of circuits. Basically, testability refers to the following two qualities.

(1) Controllability

Controllability indicates the ease of setting values for internal circuits.

(2) Observability

Observability indicates the ease of observing values in internal circuits.

Several variations of these methods have been proposed as quantification methods, but these methods are the most often used for expressing separate values of combination circuits and sequential circuits by setting separate indices corresponding to "0" and "1" values.

### 5.4.2 Testability methods

Various methods have been developed and proposed so far as DFT methods. The following are some widely used methods.

- (1) Ad hoc method
- (2) Separation test
- (3) Scan path test
- (4) Iddq test

**(1) Ad hoc method**

This method is not a pre-formulated method but rather seeks to improve testability by adding pins or control logic as needed for the target circuit. One ad hoc method improves controllability by adding signal input pins or control gates for testing so that it becomes possible to directly establish the circuit's internal values to a certain extent. Another ad hoc method improves observability by adding test output pins to enable direct observation of signals from within the target circuit.

**(2) Separation test**

This method uses buses or other intermediate devices to enable direct input and output corresponding to specific functions. Generally, all of the input and output pins for a particular function are connected via a bus and a select signal is used to specify the function to be tested. The specified internal function can be directly tested independently from other internal circuits.

**(3) Scan path**

Scan path testing uses flip flops as shift registers rather than as ordinary logic so that values can be set to the target circuit's internal flip-flops directly via test input pins without affecting the circuit's internal logic and flip-flop values can be directly observed from test output pins.

Although there are various ways to perform scan path tests, the basic theme among all scan path test methods is that control signals, clock signals, etc. are used to switch the target circuit between normal operation mode and scan path mode in which shift operations are performed to enable setting and observation of values.

The "full scan" method uses all of the target circuit's flip-flops as scan path flip-flops and the "partial scan" method uses only some of the flip-flops in this way. One advantage of the full scan method is that test patterns can be automatically generated. When using the partial scan method, note with caution that the test patterns which are obtained do not always have an adequate failure detection rate.

**(4) Iddq tests**

Iddq tests are techniques that are basically used for CMOS ICs. Iddq tests take advantage of the fact that, when a normal CMOS IC is in a steady state (a state in which its values do not change) it has only a very small through current, but when a defect occurs the circuits in the defective area become activated and have a large through current, which can be detected by tests that measure the supply current. Recently, Iddq tests have been increasingly used as a way to boost the failure detection rate. Since Iddq testing involves relatively little overhead (elements added for testing, etc.) it has gained attention as an inexpensive test method.

### **5.4.3 Application of DFT methods**

As mentioned above, there are various DFT methods. From the viewpoint of obtaining adequate fault coverage and reducing overhead costs of the circuit area (gate counts), and so on, the optimum method should be selected. As a general example, general circuit testing methods such as scan path tests are used to test random logic blocks that differ according to the design. For devices such as analog multi-function ICs, separation tests and ad hoc methods are used. In addition, Iddq tests are generally used to improve overall fault coverage for CMOS circuits.

### **5.4.4 Tools for test**

Currently, several types of CAD tools are being developed and used to implement the kinds of tests described above. Typical examples of tools that implement design for test methods include CAD tools for automatic configuration of circuits, ATGs (Automatic Test Generators) to generate test patterns, and fault simulation methods to measure the failure detection rates of generated test patterns. It is important to use these tools effectively since, for quality assurance purposes, high failure detection rates are required of test patterns used for mass-produced devices.

Test program auto generation tools for testers have been developed to enable logic IC test controls, including these test method controls, and settings to be made from an IC tester. The program check lists for every function, etc. is utilized for the analog IC. The test program auto generation tools and program check lists play an important role in improving quality assurance through the use of more suitable settings (such as for measurement items and measurement conditions) and in promoting the standardization of test programs.

## 5.5 FMEA

FMEA (Failure Mode and Effect Analysis) is a method whose purpose is to detect areas of incomplete design and manufacturing process or other latent defects.

This method consists in hypothesizing and enumerating the potential failure modes, potential failure influences, and potential cause mechanisms of each element making up a system. If a failure in a specific mode occurs, how the entire system is affected is classified and ranked by occurrence, influence, detection, and importance. In this way, the failures having the most serious influence can be found, countermeasures can be taken, and failures in this mode can be prevented.

The FMEA method is also useful for analyzing reliability problems in new products or small-lot products for which quantitative predictions of reliability are difficult.

The implementation steps for FMEA are described below.

- (1) Make a list of the elements that configure the overall system.
- (2) Hypothesize the failure modes that are expected to occur due to component failures.
- (3) Hypothesize the effects on the sub system and overall system.
- (4) Evaluate the extent of the effects.
- (5) Study effective preventive measures.

FMEA worksheets are used to facilitate these implementation steps. (Table 5-4 shows an example of worksheet.)

Table 5-4. Example of FMEA Worksheet

Component and Function or Work		Potential Failure Mode	Potential Failure Influence	Potential Failure Cause Mechanism	Evaluation Point				Processing Contents (Process Management)
Process	Function				Occurrence	Influence	Detection	Importance	
Dicing	Separating wafer	Chip crack Chipping	Characteristics fail Characteristics degradation	Blade degradation Wafer adhesive is soft and chip moves.	1 2	4 5	1 3	4 30	Blade wear control Appearance check Illuminate UV before dicing
Mounting	Gluing chip to lead frame	Chip peel-off	Open	Temperature low Load few	1	5	1	5	Periodically temperature measurement Periodically load measurement
		Chip crack	Characteristic fail	Pressure pin degradation	2	4	1	8	Periodically check of pin shape
Bonding	Connecting chip electrode to frame with Au wire	Peel-off at points A and E	Open	Temperature low Load few	1	5	1	5	Periodically temperature measurement Periodically load measurement Wire strength measurement
		Improper bonding position	Short	Incorrect recognition	2	5	1	10	Appearance check
Mold sealing	Sealing chip with resin	Not replenished	Incorrect appearance	Projection time Mold temperature	1	4	1	4	Start-up check Periodically temperature measurement Appearance check
		Wire flow	Short	Projection time Mold temperature	1	5	2	10	Start-up check Periodically temperature measurement X-ray check
		Lead deformation	Short	Wear of plunger head Scar on plunger head Lead frame	2 2 6	7	2 2 6	28 28 252	Wear control Appearance check X-ray check Lead frame structure change
Solder plating	Plating lead	Plating thickness	Solderability	Current Liquid composition	1	3	2	6	Periodically inspection Periodically analysis Plating thickness check
Marking	Marking element	Incorrect marking	Mixing	Mistake by worker	1	5	1	5	Appearance check Detection by sensor