

CHAPTER 2 RELIABILITY OF SEMICONDUCTORS 52

- 2.1 Approach to Reliability52
 - 2.1.1 Definition of reliability52
 - 2.1.2 Reliability of semiconductors53
 - 2.1.3 Activities to improve reliability54
- 2.2 Reliability Testing56
 - 2.2.1 What is reliability testing?56
 - 2.2.2 Reliability test methods56
 - 2.2.3 Accelerated life testing58
- 2.3 Failure Rate Prediction Methods63
 - 2.3.1 Concept of failure rate63
 - 2.3.2 Failure rate prediction methods63
 - 2.3.3 Prediction methods used at Compound Semiconductor Devices Division64
 - 2.3.4 Prediction method from MIL-HDBK-21766

CHAPTER 2 RELIABILITY OF SEMICONDUCTORS

2.1 Approach to Reliability

2.1.1 Definition of reliability

According to the Japanese Industrial Standards (JIS Z 8115, Glossary of terms used in reliability), reliability is defined as characteristics that enable an item to perform its required functions under the stipulated conditions and for the stipulated time period. In other words, reliability resides in characteristics that enable a product to operate without malfunctions for the intended use period, which refers to a product's quality over time.

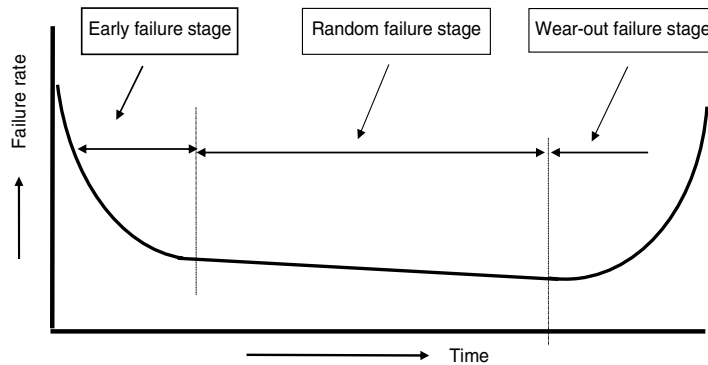
Quantifiable yardsticks such as the reliability rate, failure rate, and mean time to failure (MTTF) are used to measure reliability.

2.1.2 Reliability of semiconductors

To evaluate the reliability of an electronic system, reliability information on the components used in that system is important. Failure rates are often used as an index for reliability. A failure rate indicates how often a failure occurs per unit time, and failure-rate values generally change over time as shown in Figure 2-1.

Each failure area in this figure is explained below.

Figure 2-1. Time-Related Changes in Failure Rate



- **Early failure stage:** During this stage, failures occur at a high rate following the initial operation of semiconductor devices. They occur very soon and thus the failure rate declines rapidly over time. This is because the potential failures that could not be removed through a selective process are included and surface in a short time if a stress such as temperature or voltage is applied after use of the device is started. In the case of semiconductors, these failures are usually due to defects that could not be removed during production, such as micro dust collecting on the wafer, or to material defects.
- **Random failure stage:** When early failures are eliminated, the failure rate drops to an extremely low value. However, there is always the possibility of a potential failure accidentally occurring after a long time. Consequently, the failure rate never decreases to zero. It is almost constant because failures occur sporadically.
- **Wear-out failure stage:** During this stage, failures occur with increasing frequency over time and are caused by age-related wear and fatigue. In the case of a semiconductor device, electronic migration or oxide film destruction (TDDB) may occur (see **CHAPTER 3 FAILURE MODES AND MECHANISMS**).

The failure rate is generally expressed in (fit = 10⁻⁹/h). This indicates the number of failures per unit time. In general, the mean failure rate of a semiconductor device per unit time is calculated with the following expression.

$$\text{Mean failure rate} = \frac{\text{Total number of failures in given period}}{\text{Number of base devices} \times \text{Operation time}}$$

According to this expression, 1 (fit) is expressed as follows.

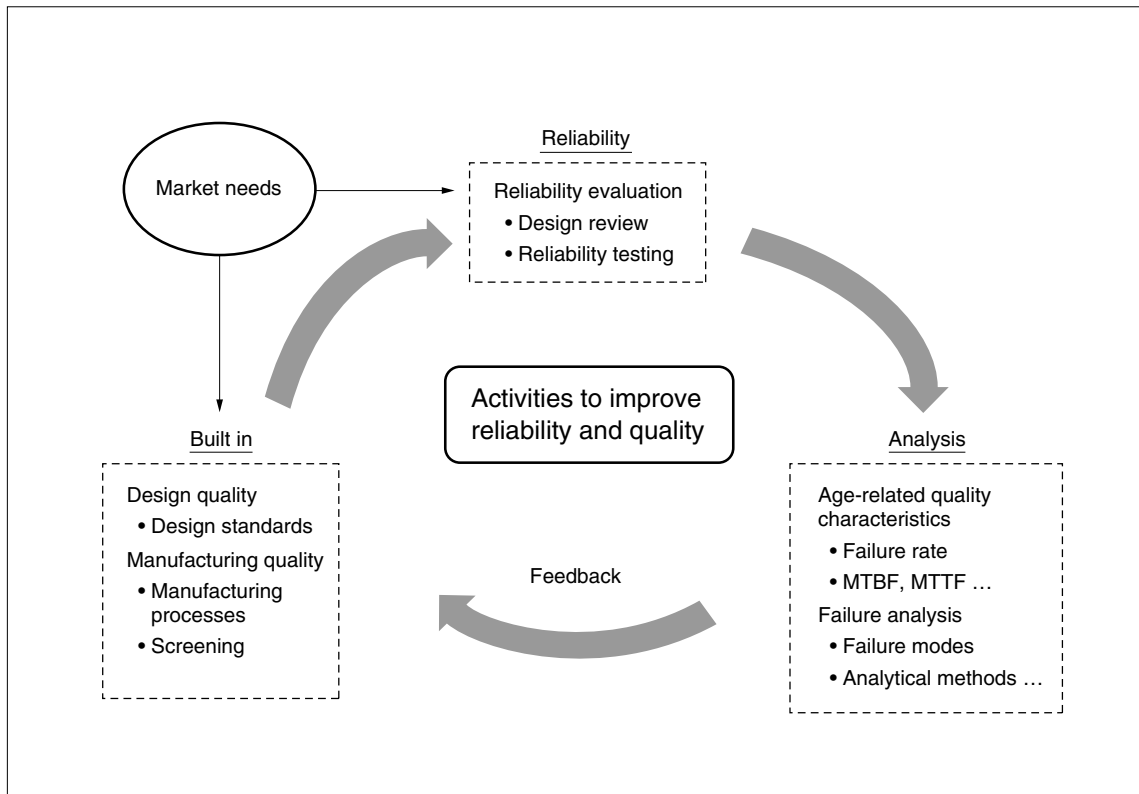
$$1 \text{ (fit)} = \frac{1 \times 10^9}{\text{Number of bases: } 100000 \times \text{Operation time: } 10000 \text{ hours}}$$

In other words, 1 (fit) is equivalent to a failure of one device per 100,000 devices operated for 10,000 hours.

2.1.3 Activities to improve reliability

As a manufacturer of electronic components, it is essential that Compound Semiconductor Devices Division perform a cycle of activities to improve reliability. This cycle is illustrated in Figure 2-2.

Figure 2-2. Cycle of Activities to Improve Reliability and Quality



(1) Understanding market needs, customers’ reliability requirements, and use conditions

When developing new products, it is important to understand market needs, customer’s requirements and use conditions, information about the use environment, etc. An understanding of such information should be reflected in product designs and manufacturing processes. Specific information may include the customer’s reliability requirements, use conditions such as the ambient temperature, humidity, and power supply voltage, and environmental conditions such as vibration, static electricity, and application of overvoltage. Information from customer complaints can also be used to gain insights into market needs.

(2) Creation of reliability

Design for reliability is performed to ensure that an understanding of needs (market needs, customer needs, etc.) is reflected in the design of products. Key elements include parameter design, quality and function deployment, FMEA, and FTA methods, etc.

(3) Reliability evaluation

Design reviews are performed to confirm and evaluate the suitability of product designs. They verify whether or not a design complies with the relevant design standards, whether or not the selection standards and the evaluation are appropriate when using new materials or new processes. The reliability evaluation process also includes collective measures against abnormalities. In addition, the design review must also confirm whether or not the expected level of reliability has been built into prototype samples. Usually, accelerated tests are used in reliability testing to reduce evaluation time and costs. Acceleration conditions in which hypothesized failure matches to the market results should be determined.

(4) Analysis of evaluation results

Failure analysis methods are used to look for causes of failures that occur during reliability testing or that are described in complaint reports. Here, the objective is to provide feedback to the design and screening processes by determining which mechanisms cause problems in which mode. Also, the reliability test results can be used with statistical methods to estimate a product's age-related quality (failure rate, etc.).

(5) Feedback from results

To prevent failures, the product's design and manufacturing processes must be reviewed and revised. If revisions need to be extended to other product as well, the revisions must be worked into the standards (design standards, manufacturing process standards, etc.) that apply to those products.

The above steps are cycled through in order to bring ever higher levels of reliability to product designs.

This chapter explores some of the above-mentioned topics that are important for verifying and improving reliability. Specifically, reliability testing, failure modes and failure analysis (including failure analysis devices) are described in this chapter.

2.2 Reliability Testing

2.2.1 What is reliability testing?

Customers naturally expect semiconductor devices to perform the required functions from the moment they are first used, and they also expect the devices to function without failure throughout the expected use period. This brings us back to the above-mentioned definition of reliability as characteristics that enable an item to perform its required functions under the stipulated conditions and for the stipulated time period.

According to JIS Z 8115 (Glossary of terms used in reliability), reliability testing is defined as a general term referring to tests that determine reliability and tests that evaluate the suitability of reliability. In other words, reliability testing is intended to confirm whether or not reliability required by customers are present in semiconductor devices.

2.2.2 Reliability test methods

(1) General

The objective of reliability testing is to confirm a semiconductor device's fault-free operation and to estimate its useful life by exposing the device to accelerated or marginal stress based on the amount of stress (thermal stress, mechanical stress, electrical stress, etc.) that the device is estimated to undergo during manufacture, shipping, and use.

To achieve this objective, it is important even as early as the semiconductor device planning stage to fully understand customer needs and the range of market applications so as to establish appropriate quality and reliability levels, which can be confirmed via appropriate reliability tests.

Reliability tests are performed under various stress conditions that are based on hypothesized stress conditions during manufacture, shipping, and use, and various semiconductor device testing methods have been standardized, such as in the Japanese Industrial Standards (JIS), the Japan Electronics and Information Technology Industries Association (JEITA) Standards, Military Specifications and Standards (MIL), and the International Electrotechnical Commission (IEC) Standards.

The stress received by semiconductor devices includes mechanical stress such as shock or vibration, thermal stress such as soldering temperature or ambient temperature, and electrical stress such as electrical currents or voltages. The tests that verify how resistant devices are to such stress are broadly divided into environmental tests and endurance tests.

Table 2-1 lists some typical categories of reliability tests conducted at Compound Semiconductor Devices Division.

Table 2-1. Example of Reliability Test Categories for Semiconductor Devices

Test Category		Relevant Standards		Test Method and Test Conditions	Examples of Detectable Failure Mechanisms	
		ED-4701	MIL-STD-883			
Environmental tests	Thermal environmental tests	Resistance to soldering heat	301 302	–	260 ±5°C for 10 seconds	Package crack Chip crack Bonding falling off
		Temperature cycle	105	1010 Condition C	One cycle: test at below minimum temperature for 30 minutes, then test at above maximum temperature for 30 minutes. 10 cycles	
		Thermal shock	307	1011 Condition C	100°C for at least 5 minutes 0°C for at least 5 minutes 15 cycles	
	Mechanical environment tests ^{Note 1}	Variable frequency vibration	403	2007 Condition A	Peak 20 G, 20 to 2,000 Hz 4 times for 4 minutes in each direction (X, Y, and Z)	Package crack Chip crack Bonding falling off
		Shock	404	2002 Condition B	1,500 G 3 times for 0.5 ms in each direction (X, Y, and Z)	
		Constant acceleration	405	2001 Condition D	20,000 G 1 time for 1 minute in each direction (X, Y, and Z)	
	Solderability		303	2003	215 ±5°C or 245 ±5°C for five seconds, with flux	–
	Terminal strength (bending)		–	2004 Condition B2	Three times for randomly selected pins, using rated weight and bending to 90 (±5) degrees	–
	Endurance tests	High temperature storage		201	1008	Test at above maximum temperature for at least 1,000 hours
Continuous operation ^{Note 2} or high temperature bias		101	1005	T _A : 125°C or above for at least 1,000 hours Type of test and load conditions are determined by test.	Ion contamination Oxide layer damage Broken junctions	
Intermittent operation ^{Note 3}		106	1006	Access via continuous operation and ON/OFF cycles are determined by test.		
Humidity resistance		102	–	T _A : 85°C, RH: 85% for at least 1,000 hours When there are applied voltage and load conditions, they are determined by test.	Aluminum corrosion	
Pressure cooker test (PCT) ^{Note 4}		–	–	Exposure to hot vapor (125°C, RH 100%) having 2.3 barometric pressure for at least 96 hours	Aluminum corrosion	
Temperature cycle		105	1010	One cycle: test at below minimum temperature for 30 minutes, then test at above maximum temperature for 30 minutes. 100 cycles or more	Package crack Chip crack Aluminum slide	

Notes 1. Applicable for hermetically sealed packages

2. Select either continuous operation or intermittent operation according to device relevant specification.

3. Applicable for mold-resin type packages

4. Applicable only for certification testing

(2) Environmental tests

These environmental tests use simulations of models wherein a semiconductor device that is undergoing stress fails when limit values are exceeded. Environmental tests are broadly divided into thermal environmental tests and mechanical environmental tests.

<1> Thermal environmental tests

The objective of thermal environmental tests is to confirm a mounted semiconductor device's resistance to the thermal stress conditions it is under during its use period. Using thermal stress equivalent that applied during solder mounting, the samples are tested under a series of thermal variation stress conditions. The maximum rated soldering temperature is used during soldering.

<2> Mechanical environmental tests

The objective of mechanical environmental tests is to confirm a manufactured semiconductor device's resistance to the mechanical stress conditions it is under during shipping, mounting, and use. The amount of stress applied is estimated as being greater than the amount actually experienced during shipping, mounting, and use.

(3) Endurance tests

Endurance tests use simulations of models wherein a semiconductor device is exposed to stress conditions that are below the limit values but that are applied over time to test for age-related failures.

Semiconductor devices generally have a long useful life, which makes it very difficult to test endurance under ordinary use conditions. Therefore, when stress that exceeds the rated value is applied to a semiconductor device, age-related deterioration is accelerated so that the device's useful life can be measured in a relatively short time. This type of test method is called accelerated life testing.

2.2.3 Accelerated life testing

(1) General

Accelerated life testing is used to predict the device's useful life and failure rate in a short testing period.

Accelerated life testing exposes a semiconductor device to stress conditions that are harsher than during actual use, the speed of reactions to failure events is also accelerated, which speeds up aged-related deterioration and shortens the testing period. However, correct life estimations cannot be made unless selected test methods have failure modes that are similar to the failure modes under actual use conditions.

(2) Acceleration using thermal stress

In many cases, the Arrhenius model is used to represent physical and chemical events related to deterioration of semiconductor devices. The Arrhenius model is a basic chemical reaction model for temperature-dependent failures, and in this case it is applied to estimate the useful life of semiconductor devices which are subjected accelerated life tests that use thermal stress.

Life (L) is expressed as follows in the Arrhenius model.

$$L = A \cdot \exp\left(\frac{E_a}{kT}\right)$$

Where,

L: Life

A: Constant

E_a: Activation energy [eV]

k: Boltzmann's constant (8.62×10^{-5} [eV/K])

T: Absolute temperature [K]

This equation expresses the relation between temperature and product life, so that if the failure mode is the same, the relationship between life ($\ln L$) and temperature ($1/T$) values obtained from life testing will be as shown in Figure 2-3, which enables product life under actual temperature (T_0) to be estimated. The type of diagram shown in the figure is called an Arrhenius plot. The slanted line in Figure 2-3 represents the activation energy (E_a).

Figures 2-4 and 2-5 show changes over time that occur during accelerated life testing. As can be seen in Figure 2-4, changes in characteristics occur at temperature values of 337°C, 295°C, and 259°C. The graph of changes over time indicates a rapid rate of acceleration. Figure 2-5 shows an Arrhenius plot of the test results. The angle of the line indicates an activation energy (E_a) of approximately 1.5 eV. This activation energy and the temperature-dependent changes over time during testing can be used to estimate the changes that will occur under actual use environment temperatures.

Figure 2-3. Arrhenius Plot (Relation Between Life and Temperature)

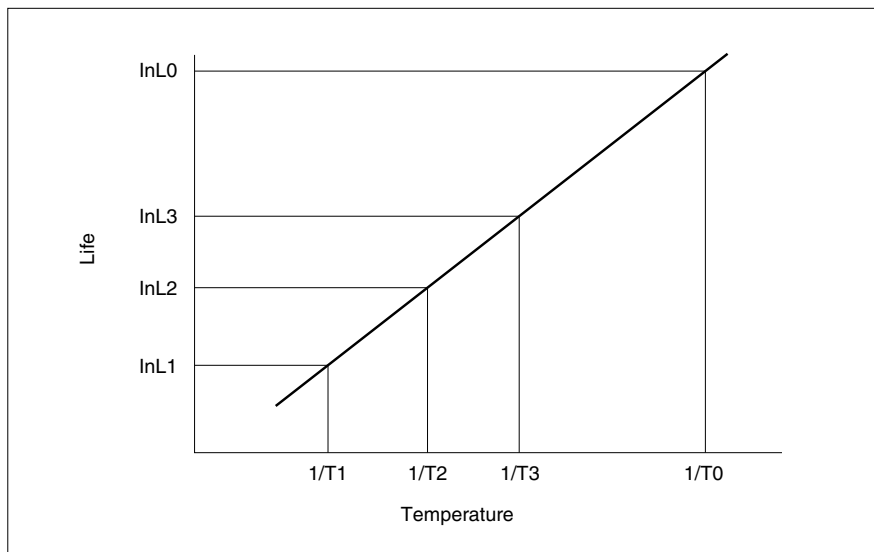


Figure 2-4. Graph of Age-Related Changes

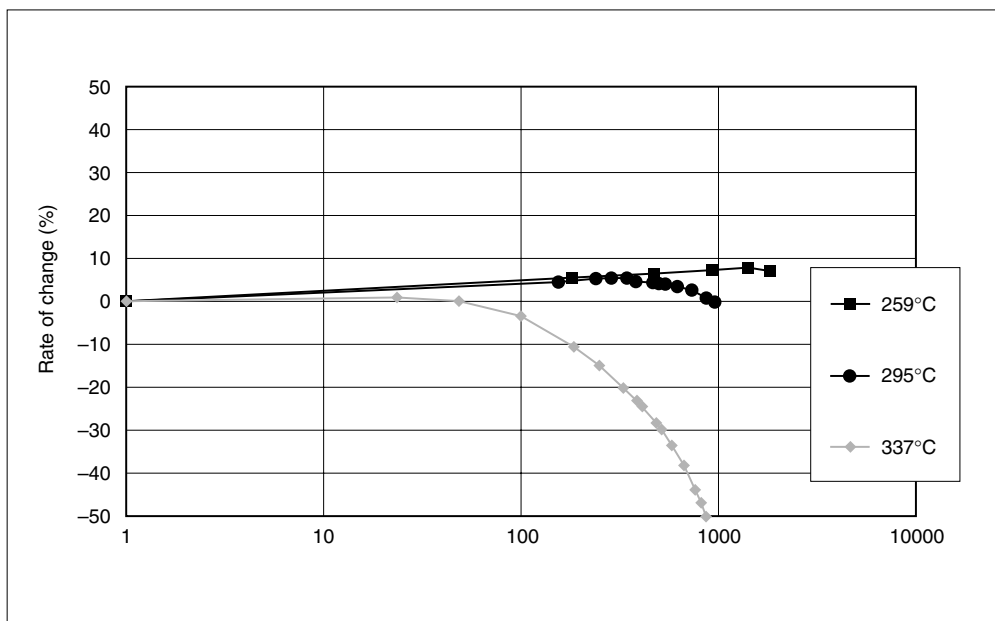
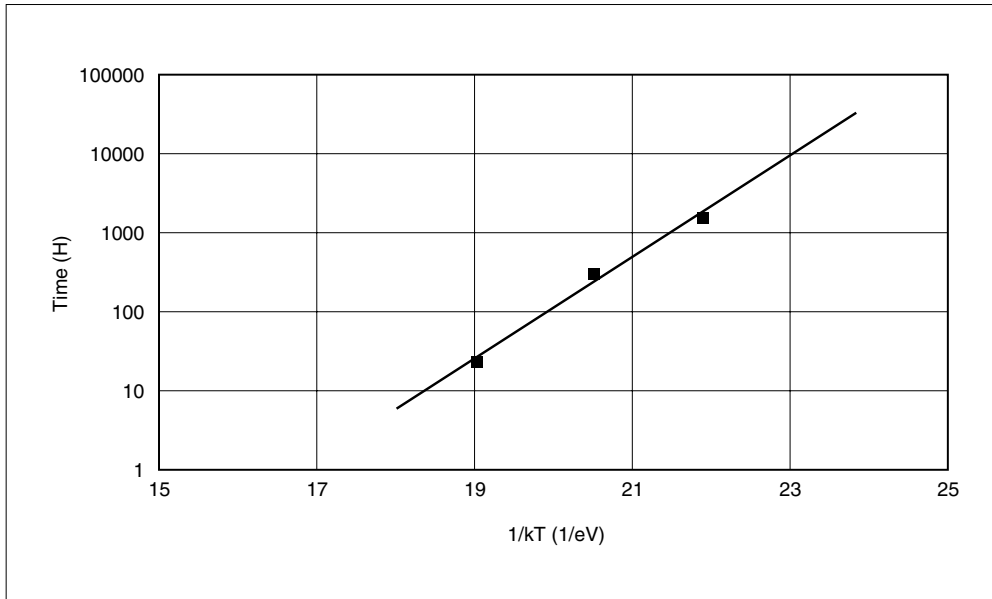


Figure 2-5. Arrhenius Plot



(3) Failure modes based on higher temperatures

Failures that ordinarily occur in semiconductor devices can be accelerated by higher temperatures. However, even when the failure modes are the same, there are various failure mechanisms that can occur. Since the reaction speed varies among different failure mechanisms, the activation energy also varies. Therefore, the failure mechanism can be considered an analog of the activation energy, which enables life estimations to be made.

Table 2-2 lists typical failure modes, failure mechanisms, and activation energy values related to higher temperatures in semiconductor devices.

Table 2-2. Typical Failure Modes, Failure Mechanisms, and Activation Energy Values

Failure Mode	Failure Mechanism	Activation Energy (eV)
Vt variation	Ion contamination	1.0 to 1.4
	Slow trapping	1.0 to 1.5
Short	Oxide layer damage	0.3
Open	Electromigration in wiring	0.5 to 1.0
	Au-Al intermetallic compound	0.8 to 1.0
	Corrosion of Al wiring	0.5 to 1.0
Increased leakage current	Generation of inversion layer	0.5 to 1.0

(4) Acceleration based on humidity

Recently, mold plastic semiconductor devices have come into wide use. The reliability of mold resin type semiconductor devices depends greatly on the device's humidity resistance, and various test methods are used to provide an early evaluation of reliability. Typical testing methods are described in Table 2-3. At Compound Semiconductor Devices Division, high temperature/high humidity bias testing (or storage testing) and pressure cooker testing (PCT) are performed to check humidity resistance.

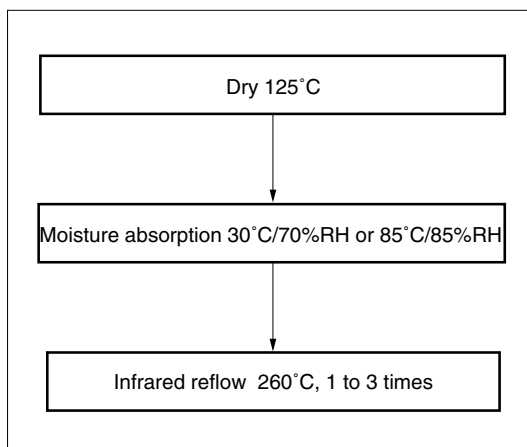
Humidity resistance testing is prone, however, to problems such as variation in reproducibility and failure modes that differ from actual use results, and consequently extra caution is required when implementing humidity resistance tests.

In addition, recent semiconductor devices are mainly surface mount devices (SMDs), which are becoming smaller, thinner. For these devices, thermal stress during mounting and moisture absorption in resin during storage are two factors that cannot be ignored. To correctly simulate actual use, mounting stress is applied as shown in Figure 2-6, in a preprocess that is part of humidity resistance testing.

Table 2-3. Main Moisture Resistance Testing Methods

Testing Method	Test Conditions
High temperature, high humidity storage test (HHT)	85°C/85% RH
Pressure cooker test (PCT)	125°C/100% RH
High temperature, high humidity bias test (HHBT)	85°C/85% RH Bias is applied
Unsaturated pressure cooker bias test with bias	130°C/85% RH Bias is applied

Figure 2-6. Examples of Simulation of Soldering Heat



(5) Screening

Screening is implemented to eliminate early failures. In one type of screening, a suitable amount of stress (not enough to wear down or damage a device that has no latent defects) is intentionally applied to products to wear down latent defects so that they can be detected and removed by appropriate tests performed afterward. In another type of screening, defective products are detected and removed at a suitable stage during manufacturing and without having to apply stress. These screening concepts are described in Figure 2-7. When selecting an appropriate type of screening for a product, a great deal of consideration must be given to the product's applications, the required quality level, as well as the product's design, structure, and fabrication method. In addition, the screening process must not have an adverse impact on nondefective products. Table 2-4 lists some typical screening methods being used today. Suitable screening methods are selected and applied for the actual products based on the required quality level and/or required specifications.

Figure 2-7. Variation in Quality Level Due to Screening

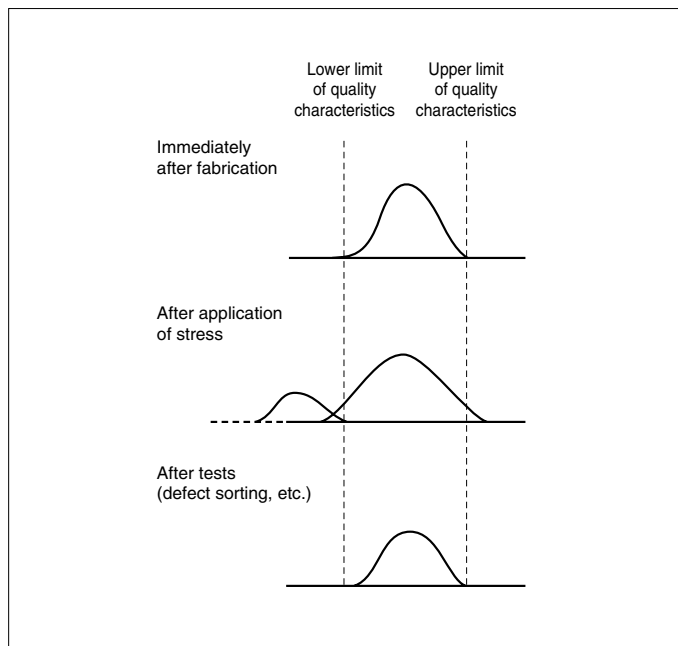


Table 2-4. Typical Screening Methods

Type	Screening Method	Expected Failure Removal
Non-stress methods	Visual inspection before sealing	Die surface defects, bonding wire defects, etc.
	Visual inspection after sealing	Package surface defects, damage, etc.
	X-ray fluoroscopy	Bonding wire distortion, die bond and eutectic alloy defects, etc.
Thermal stress methods	Temperature cycle	Die bond, package defects, hermetic sealing defects, etc.
	Thermal shock	Same as above
	Low-temperature test	Effect of hot carrier, variation in electrical characteristics, etc.
Mechanical stress methods	Drop impact	Die bond, bonding wire and package defects, etc.
	Constant acceleration	Same as above
	PIND	Foreign particles in cavities within packages
Electrical stress methods	Burn-in	Defects inside the die, such as micro particles, dirt, and thin-film defects
	Application of high voltage	Inadequate insulation layer, inadequate voltage resistance in circuit, etc.

2.3 Failure Rate Prediction Methods

2.3.1 Concept of failure rate

Difference between failure rate and defect rate

Where there are r defects in a population of n units, the defect rate is expressed as r/n . The defect rate does not take time lapse into consideration, and indicates the ratio at which defects exist. In contrast, the failure rate indicates the rate at which failures occur per unit time, and varies over the time during which the device or system is operated. It is therefore an index intrinsically different from defect rate.

2.3.2 Failure rate prediction methods

(1) Failure rate estimation method

The failure rate of a general semiconductor device is considered to be about several to several 100 fit, which is lower than for other electronic components such as capacitors and switches. It is therefore difficult to actually measure the failure rate of a semiconductor device, but there are ways to accomplish this. If the failure rate of the same device is calculated by different prediction methods, however, an error of one to two digits may occur. It is therefore important not to judge the reliability of the device based on values alone, but to also give careful consideration to the prediction method(s).

(2) Types and features of prediction

Table 2-5 lists some typical failure rate prediction methods and their features.

Table 2-5. Typical Failure Rate Prediction Methods

Method	Advantages	Caution Points
Estimation based on life testing	Reliability test data can be used. Data can be obtained under controlled conditions.	Amount of data is limited. Failures often do not occur during the fixed time test period (resulting in poor estimation accuracy). Caution is required concerning failure mode differences between tests and actual use.
Estimation based on market results	Raw data is obtained.	To get an accurate grasp of the data, information on the customer's use conditions and monitoring of time to failure are required. This method is not suitable when the product is fabricated using a new process or in other cases where there are no previous market results.
Estimation based on prediction formula	Enables immediate estimations.	It is difficult to determine the prediction formula and the reliability factor coefficients. A correlation must be made periodically between prediction formula results and life testing results and market results.

2.3.3 Prediction methods used at Compound Semiconductor Devices Division

(1) Failure rate prediction methods

At Compound Semiconductor Devices Division, the following methods are used to calculate failure rates. Generally, estimates are performed based on trends taken from life tests and also based on prediction formulas. How to estimate a failure rate using a typical life test is explained below.

[Failure rate estimation based on life testing]

Even though the product functions are specific to each product, if the process (design rule) is the same, the design quality can be considered as roughly equivalent. When life testing results for product models that use the same process are accumulated, it becomes possible to estimate their failure rate. This calculation is basically done using the following formula.

$$\gamma_{b2} = P_2 / (N_2 \times T_2 \times A) \times (60\% \text{ confidence level})$$

where γ_{b2} : Failure rate (base on life test results)

P_2 : Total number of manufacturing defects

N_2 : Total number of target devices shipped

T_2 : Average operation hours (1920 h)

A : Rate of acceleration

(2) Calculation of failure rate for specific use conditions

The previous section describes failure rate calculation methods for semiconductor devices. When semiconductor devices are mounted onto a set and are operated, the failure rate must be adjusted to take the use environment into account.

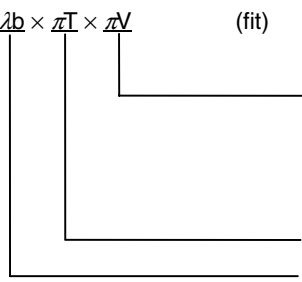
To do this, the semiconductor device's environmental conditions (such as temperature condition) are hypothesized and new failure rates are calculated for customers as shown in Table 2-6. The results of these calculations are used as the failure rates for actually used semiconductor devices.

Table 2-6. Failure Rate Values Reflecting Use Conditions

The device's failure rate (λ) is determined based on the device-specific basic failure rate (λ_b) and the use conditions. After considering the hypothetical use environment, the failure rate can be calculated via the following steps.

- Failure rate estimation formula (λ) (failure rate during random failure stage)

$$\lambda = \lambda_b \times \pi T \times \pi V \quad (\text{fit})$$



- <2> Power supply voltage parameter
Applicable only for silicon transistors, FETs, and transistors with internal resistor
($\pi V = 1$ for products other than above)
- <1> Temperature parameter
Basic failure rate

- <1> Temperature parameter (πT)

$$\pi T = \exp \left(11600 \times E_a \times \left(\frac{1}{273 + 55} - \frac{1}{273 + T_A(j)} \right) \right)$$

Ea: Activation energy

T_A: Ambient temperature during use (for IC)

T_j: Junction temperature during use (for discrete device)

Expressed as T_{A(j)} in above formula

πT Reference Chart (when E _a = 0.7 eV)										
T _A (j)	40	55	60	65	70	75	80	90	100	110
πT	0.31	1	1.45	2.08	2.95	4.15	5.77	10.9	19.8	34.99

- <2> Power supply voltage parameter (πV) – Applicable only for silicon transistors, FETs, and transistors with internal resistor

$$S = \frac{\text{Used power supply voltage (V}_{CE} \text{ or V}_{DS})}{\text{Absolute maximum rated voltage (V}_{CEO} \text{ or V}_{DSS})}$$

When $S > 0.2$, $\pi V = \exp(2.86 \times S - 2.29)$

When $S \leq 0.2$, $\pi V = 0.18$

(Calculation standard)

- Reliability level: 60%
- Basic temperature = 55°C
- Used under recommended conditions

2.3.4 Prediction method from MIL-HDBK-217

MIL-HDBK-217 (Department of Defense Military Handbook: Reliability Prediction of Electronic Equipment) was developed by the Pentagon with the assistance of the Department of the Army, various other Federal agencies, and industry representatives.

The purpose of creating the MIL-HDBK-217 handbook is to establish a uniform methodology for predicting the reliability of military electronic equipment and systems and to provide a common basis for reliability predictions performed at the acquisition program stage for military electronic equipment and systems. This handbook also establishes a common basis for comparing and evaluating reliability predictions of related or competing designs.

The data in the MIL-HDBK-217 handbook has been collected as field usage data for vast numbers of military electronic equipment that is purchased under MIL standards. Since compliance with MIL-HDBK-217 has been established by the Pentagon as a requirement in the military electronic equipment that it purchases, a safety coefficient must be fully taken into account for each factor. Consequently, the calculated failure rate for such devices tends to much greater than when using ordinary reliability prediction methods.

When a comparison is made between failure rates calculated using Compound Semiconductor Devices Division's methods and failure rates calculated using MIL standard methods, the failure rate values for MIL are from 10 to 100 times greater than those for Compound Semiconductor Devices Division.