

NEW ASIC PROCESS TECHNOLOGY MAKES EMBEDDED DRAM PRACTICAL CHOICE FOR HIGH-PERFORMANCE APPLICATIONS

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The advantages of embedding large blocks of memory into a system-on-a-chip (SoC) ASIC have become increasingly clear in the face of growing performance demands for many applications. However, because of manufacturing and performance constraints, embedded memory has been available for a limited number of applications only. Now a fabrication process compatible with DRAM and logic requirements makes embedded DRAM practical on a much wider scale than ever before. This new approach is boosting the performance of applications ranging from game consoles to advanced communications equipment.

To make the right choices for specific applications, designers must understand the tradeoffs associated with various embedded memory options. This white paper describes those tradeoffs and explains how NEC Electronics has transformed embedded DRAM options with a new process technology that reduces the number of fabrication steps and improves system performance by making the embedded DRAM function like SRAM (that is, with single-cycle access) while consuming far less power and requiring much less die area.

ARRAY OF HIGH-PERFORMANCE APPLICATIONS

The application area that stands to benefit most from the use of embedded DRAM is communications, if only because of the large number of roles that embedded DRAM can fill. For example, NEC Electronics is seeing high-speed random access embedded DRAM blocks go into framers, network processors and traffic-management ASICs in 10 Gbps (OC-192) and 40 Gbps (OC-768) applications. In page mode, NEC Electronics eDRAM can replace external DRAM for look-up tables and thus eliminate problems caused by jitter and power budgets. Traditionally, these devices have relied on embedded SRAM along with buffer memory and/or discrete DRAM/SRAM. The former is expensive and power-hungry, while the latter limits performance by requiring packets to be moved between chips. Embedded DRAM overcomes the limitations of both embedded SRAM and discrete DRAM/SRAM, as described later.

In other application areas, NEC Electronics eDRAM has been used in a graphics controller chip for a popular game console. This particular ASIC contains two large blocks of embedded DRAM generated by orientation-free macros, where the blocks were rotated as needed to optimize the chip's layout. The flexible layout enabled the metal on the fifth and –higher layers to be routed over the top of the eDRAM blocks, which had exceptionally fast random access time—less than 6.17 ns (0.18 μ m technology). NEC Electronics has fabricated several million of these chips.

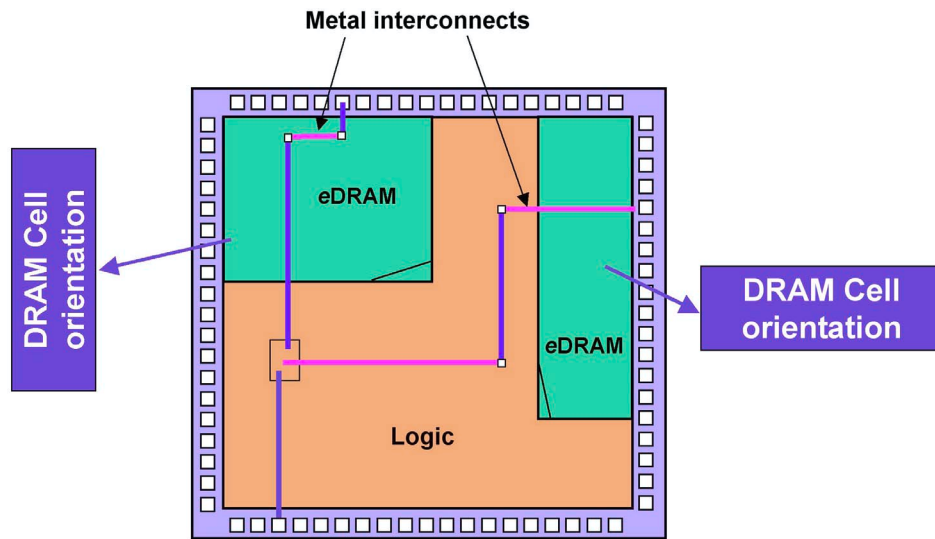


Figure 1: Chip layout with orientation-free eDRAM blocks

In addition to enabling multi-gigabit-per-second throughput, NEC Electronics eDRAM is ideal for compact designs with modest power dissipation in office, industrial equipment and lightweight electronic devices.

EMBEDDED MEMORY IN SoC DESIGN FLOW

Since today's designs are driven by the need for more and more functional blocks on a single chip designed within tight design cycles, engineers must take advantage of existing intellectual property (IP). At the same time, designers are spending more time on refining a chip's architecture to best support the end application. Thus, decisions about an ASIC's functional blocks are made before project commitments are finalized. These architectural decisions concern major IP blocks, buses, timing domains, routing schemes and other factors. By making these decisions early in the design flow, a company minimizes the risks associated with project implementation, scheduling and time to market before committing financial and engineering resources to the project. To give designers maximum flexibility in

making these and many other decisions, ASIC vendors must support a range of design flows, from the traditional ASIC hand-off flow to methodologies that allow more designer involvement in physical design.

Although chip densities have increased (following Moore's law), the availability and broad concept of the functional blocks have not changed much. The blocks consist of IP with specialized I/Os, digital signal processing (DSP) functions and some control logic. Most designers have used embedded memory sparingly, but embedded DRAM has expanded memory choices so that multi-megabit memory devices can be included easily, along with the more traditional IP. Most of this memory traditionally has been off-chip because embedded memory failed to meet designers' requirements.

Designers have long wanted SRAM functionality with DRAM area and power consumption. With the advent of this type of memory, 50 percent or more of an SoC's die will consist of embedded memory. Now that designers increasingly deal with low-power needs and mixed-signal designs, each designer must decide whether a given SoC will benefit from the most power-stingy and least noisy embedded DRAM. Usually the answer will be "yes" for a wide range of applications, including general-purpose uses for graphics and PC functions, as well as storage and buffer memory for multimedia and telecommunications applications. True system-level integration of complex digital and mixed-signal designs requires the integration of DRAM along with logic functions.

In many systems, designers use FPGAs rather than ASICs to get fast turnaround for custom logic. The cost of using FPGAs is extreme, however, with silicon utilization averaging about 40 to 45 percent. For systems manufactured in significant volume, companies can reduce costs dramatically by converting the FPGA designs to SoCs and then integrating discrete memory at the same time.

MANUFACTURING CONSIDERATIONS FOR EMBEDDED DRAM

Designs with multi-megabit memory require a careful approach to production. With memory occupying more than half the die in new designs, unique yield and fault models become dominant contributors and must be managed well.

Above 1 megabit (Mb), redundancy and repair become critical. Additionally, the importance of a built-in self-test (BIST) is paramount because it is impractical to fully test a large embedded memory at speed with direct memory access (DMA). The wide data buses needed for DMA cannot be pinned-out in an economical package.

Cost-effective, high-performance SoC designs can be realized by bringing technologies used in commodity memory together with an innovative BIST strategy. Economics also must be considered in multi-megabit embedded memory tests. Because memory must undergo stress to be tested properly, the only economical test flow requires the use of wafer tests with cell over-voltage and high-temperature conditions. This approach enables a highly accurate repair map; repairs can be made by blowing the fuses in a standard, volume repair station.

Figure 2 shows the production test flow for SoCs with multi-megabit embedded memory. This flow improves yields for a wide range of memory sizes. If the SoC consists mostly of memory, this flow can substantially improve yields compared to yields achieved with a standard logic flow.

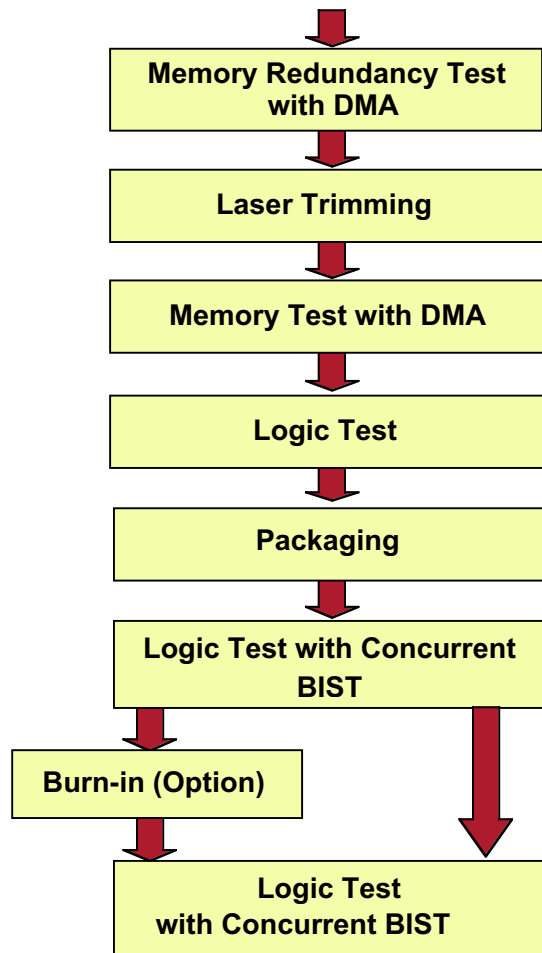


Figure 2: Production Test Flow for Merged-Logic-Type eDRAM

CHOOSING THE RIGHT MEMORY

Speed, power, area and cost are major considerations for selecting a memory architecture. The cost question is generally addressed first, usually in the form of a make-versus-buy decision. If an application requires a memory block of several megabits, the designer must choose between an off-chip solution based on discrete memory or embedded memory.

Off-chip memory has significant disadvantages because it entails a large, high-performance bus on PCB or MCM substrates such as the one illustrated in Figure 3. The use of this external bus results in undesirable multiplexing, longer delay, increased power consumption, more complicated driver designs and more complex bus arbitration schemes.

It is not surprising that designers increasingly opt for embedded memory to achieve maximum performance in throughput, form factor and power dissipation. Two types of embedded memory are usually considered: SRAM and DRAM.

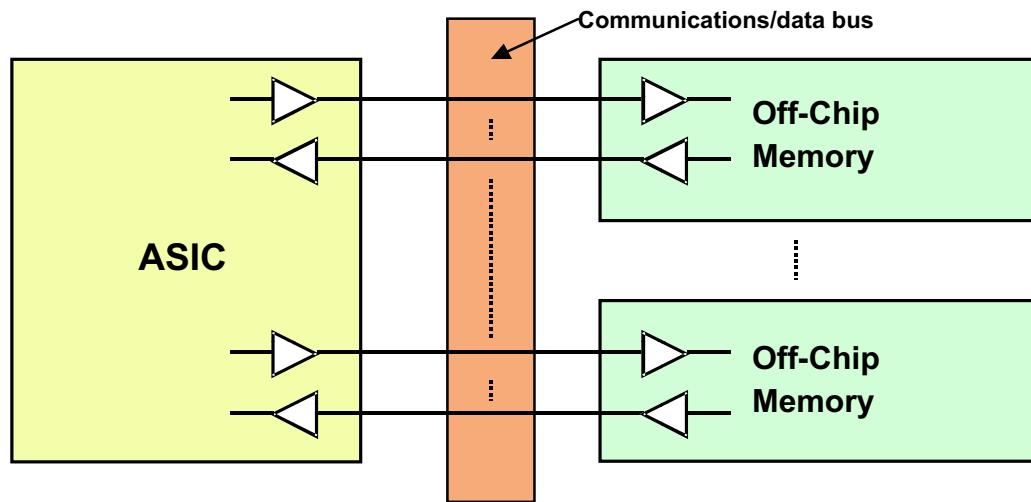


Figure 3: Off-Chip Memory with Large Performance Bus

As a reliable, proven and compiled memory technology, embedded SRAM is often the instinctive choice in embedded memory solutions. However, SRAM has drawbacks that become an issue as feature sizes shrink and integration increases. First, embedded SRAM is not dense; reasonable SRAM sizes are less than 1 Mb and require the conventional six transistors to form a single bit cell. Second, embedded SRAM dissipates more power than other alternatives. Finally, embedded SRAM has been proven increasingly susceptible to soft errors caused by the high-energy particles.

Embedded DRAM is an alternative. Designers can choose among several types of embedded DRAM made with different fabrication process techniques distinguished by their degree of compatibility with the standard CMOS logic process. Because DRAM requires the fabrication of a capacitor that is not required for logic gates, the DRAM process entails different steps. These extra steps determine the cost of adding the embedded DRAM, and in some cases the additional steps can have an adverse affect on the CMOS logic. The way the DRAM and standard CMOS processes work together is thus critically important.

Three types of embedded DRAM are generally available: DRAM-type, standard-logic (SL)-type and merged-logic (ML)-type. The DRAM-type uses the commodity DRAM process. This type of DRAM structure has high memory density resulting from a small memory cell size, but it is not suitable for high-speed applications because of its relatively low transistor performance and the relatively sparse peripheral layout design rules. Some DRAM-type processes enhance transistor performance with a large number of additional process steps, but this approach drives up the cost. Another consideration with this type of embedded DRAM is that it limits the number of metal layers, which results in inflexible ASIC layouts.

In contrast to the DRAM-type, both the SL- and ML-type embedded DRAM use the standard CMOS process but have different DRAM capacitor structures. The DRAM capacitors of the SL-type are implemented by planar capacitors (between well and gate-poly). This structure requires a relatively small number of extra process steps, but the planer capacitors must be relatively large to provide enough storage capacitance (Cs). The SL-type thus demands a lot of silicon area but still has a small storage capacitance. The small capacitance results in shorter data retention times and makes the cell somewhat more susceptible to soft errors, similar to the soft errors of embedded SRAM.

Finally, the ML-type embedded DRAM has capacitors similar to those of the DRAM-type but is based on a completely different technology from that of commodity DRAM. The ML-type takes more process steps than the SL-type, but the advantages are significant. Specifically, the ML-type process provides high-performance logic transistors (much better than the DRAM-type), a high storage capacitance for good data retention time and low soft error rate, high memory density and low power consumption. Moreover, by increasing the number of metal layers to as high as nine in today's SoC designs, the ratio of additional process steps to total process steps becomes relatively small. The ML-type's higher density also helps offset the cost of the extra process steps. Considering all the tradeoffs, the incremental performance benefits offered by the ML-type design dramatically outweigh the incremental cost.

The conventional ML-type embedded DRAM technologies have simply combined the commodity DRAM process and the standard CMOS process. The conventional ML-type technologies use two fabrication lines, commodity DRAM lines and standard CMOS lines. This approach requires a lot of back and forth of wafers between the two, and the different types of equipment require some critical process steps to be added for the reticle alignment. As a result, conventional ML-type embedded DRAM results in longer fabrication time, lower yield and higher costs. NEC Electronics now offers a unique embedded DRAM technology that can be fabricated on a standard CMOS line by changing the DRAM cell structures.

NEC ML-TYPE EMBEDDED DRAM TECHNOLOGY

NEC Electronics has been on the forefront of developing ML-type embedded DRAM as part of the company's extensive family of ASIC technologies. NEC ASICs containing large blocks of ML-type memory with a stacked capacitor structure are currently in mass production. Whether an ASIC requires modest to large amounts of embedded memory, NEC ML-type embedded DRAM offers the industry-leading choice.

In addition to the advantages already described, NEC Electronics has made proprietary improvements to the ML-type technology that benefit both the logic and memory structures on an ASIC. NEC Electronics' low-temperature, metal-insulator-metal (MIM) capacitor technology provides a good example. This capacitor is fabricated at a much lower temperature (500 degrees Celsius) than the poly-insulator-polysilicon (PIP) structure used by others. By dramatically lowering the thermal budget, the NEC process reduces thermal cycling that otherwise would cause transistor performance degradation during fabrication.

Yet another key technology advantage for NEC Electronics lies in the way the embedded DRAM capacitor structure works with chemical mechanical polishing (CMP). While conventional box-typed stacked capacitor cells leave a fair amount of height difference between the DRAM cell and CMOS logic area in a chip, the NEC cylindrical-type stacked capacitor structure dramatically reduces the height difference (Figure 4), resulting in a uniform surface over the entire chip after CMP for better yield and thus lower cost.

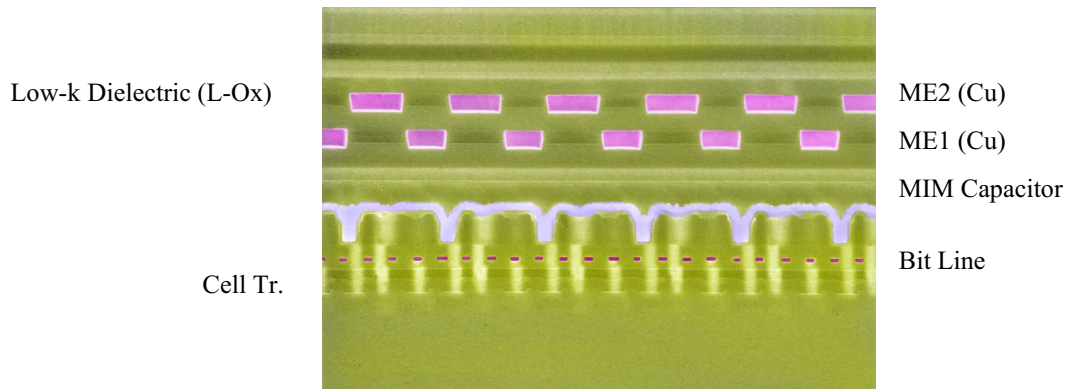


Figure 4: NEC MIM Capacitor Technology for ML-Type Embedded DRAM

Among NEC Electronics' biggest advantages is the use of metal interconnect for all bit lines in the embedded DRAM. This unique and patented process dramatically improves DRAM speed while reducing power consumption by reducing the resistance and capacitance associated with each embedded DRAM cell. The cell's node resistance is more than a thousand times lower than that of other DRAM cells. Further, because NEC Electronics' embedded DRAM uses silicide even in the DRAM cell area, the cell transistor's on-resistance is one-third to one-fourth lower than that of other embedded DRAM. These and other factors reduce the cell's resistance and capacitance delay, thus permitting much higher speeds than would be possible otherwise.

SRAM PERFORMANCE AT DRAM COST

NEC eDRAM offers DRAM-like density with SRAM-like performance, with low latency and robust speed performance (314 MHz typical at 1.2V) in 130 nm technology. The SRAM-like performance makes this device ideal for implementing high-capacity memory blocks for high-bandwidth data interfaces, for example in 10 Gbps (OC-192) and 40 Gbps (OC-768) applications, graphics accelerator and others. By bringing large, fast blocks of inexpensive memory on chip, designers easily can achieve dramatic improvements in system performance. To maximize the benefits of on-chip memory, NEC eDRAM can be implemented with a very wide data bus so that memory accesses are performed on hundreds or thousands of bits at a time.

NEC Electronics has shipped more than six million chips containing eDRAM. The benefits of the NEC-patented process are delivered to customers with little additional cost. Because increased on-chip memory often differentiates a product with higher performance and functionality, it is easy to justify a small additional cost to achieve significant added value for products.

DESIGNING WITH NEC eDRAM

Designs using the NEC eDRAM benefit from specific optimizations for reducing the noise affecting adjacent components and for operating at very low voltages. These optimizations are a must for mixed-signal SoC and battery-powered applications. NEC eDRAM is available in fully characterized and approved standard CMOS processes as well as mature CMOS processes. Moreover, NEC Electronics offers ASIC devices containing eDRAM in many different packages, including ceramic and plastic ball grid arrays (CBGA, TBGA), plastic quad flat packs (PQFP) and flip-chip solutions.

NEC Electronics' unified eDRAM and logic CMOS process technology is the result of many years of experience in the DRAM and ASIC businesses. In addition to the DRAM process optimizations, NEC Electronics has refined the design process. NEC eDRAM is part of an extensive ASIC IP library and is fully integrated into the NEC ASIC design methodology. NEC Electronics has put in place a highly versatile design flow that supports the traditional hand-off approach as well as the newer customer-owned-tooling (COT) model. Proprietary NEC tools help smooth the design path, and designers have ready access to support from the factory and engineering.

With any new development strategy, NEC Electronics recommends that customers involve NEC early in the architecture planning so that NEC support engineers can make recommendations about the best way to exploit the large embedded DRAM blocks. NEC Electronics also can answer questions about testability and manufacturing related to NEC eDRAM.

In summary, NEC Electronics' success with embedded DRAM is based on several advantages.

- The large, isolated, vertical capacitor used in NEC eDRAM is nearly immune to soft error upset.
- Density is more than five times that of embedded SRAM and two times that of SL-type DRAM.
- NEC eDRAM macros are orientation free and can be placed in SoCs in one of eight directions, allowing SoC designers to optimize floorplans for highest performance and smallest area.
- NEC eDRAM macros allow metal routing over the memory for additional layout flexibility.

- No transistor Ion degradation occurs because NEC Electronics uses low-temperature MIM capacitor technology.
- The planarity issue between logic and memory is resolved, improving yield and lowering cost.
- With new bit cell and materials in 0.13 μ m technologies, extremely high-speed designs have been characterized to offer typical operation up to 314 MHz for random access at 1.2V.
- Since the NEC eDRAM is a fully CMOS-compatible process, the eDRAM macro runs at the same voltage as the rest of the ASIC or I/Os, thus providing the designer with a single supply part offering many advantages compared to our competitors

NEC Electronics' extensive experience in commodity DRAM has given the company a head start in becoming the leader in offering embedded DRAM solutions. NEC Electronics is the only eDRAM vendor to have shipped millions of ASICs with on-chip eDRAM to boost system performance.