Manual for Using Sample Program Functions Clock Generator (V850E/IA3, V850E/IA4, V850ES/IK1, V850ES/IE2)

This manual explains the sample program functions of the clock generator for the V850E/IA4 microcontroller.

The explanations are based on usage with the V850E/IA4 microcontroller. Refer to this manual when using the V850E/IA3, V850ES/IK1, and V850ES/IE2 microcontrollers.

Caution

This sample program is provided for reference purposes only and operations are therefore not subject to guarantee by NEC Electronics Corporation. When using this sample program, customers are kindly advised to sufficiently evaluate this product based on their system before usage.

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NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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INTRODUCTION

Cautions 1. Download the program used in this manual from the NEC Electronics Website (http://www.necel.com/).

2. When using this sample program, reference the following startup file and link directive file and adjust them if as necessary.

- **Startup file: IA4_start.s**
- **Link directive file: IA4_link.dir**

Conventions The function lists are structured as follows.

Hardware name

[Function]	Function description
[Function name]	Name of sample function
[Argument]	Type and overview of argument
[Processing content]	Processing content of sample function
[Starting method]	Conditions for calling a function
[SFR(s) used]	Register name and setting content
[call function(s)]	Name and function of call function(s)
[Variable(s)]	Type, name, and overview of variable(s) used in sample function
[Interrupt(s)]	Name of function
[Interrupt source(s)]	Name
[File name]	Name of corresponding sample program file
[Caution(s)]	Caution(s) upon function usage

Product Differences The differences between the V850E/IA4 and the V850E/IA3, V850ES/IK1, and V850ES/IE2 related to the clock generator are shown below.

Item	V850E/IA4	V850E/IA3	V850ES/IK1	V850ES/IE2
Resonator	4 to 8 MHz resonator connectable (external clock input prohibited)	4 to 8 MHz resonator connectable (external clock input prohibited)	2.5 to 4 MHz resonator connectable (external clock input prohibited)	2.5 MHz resonator connectable (external clock input prohibited)
Multiplication function by PLL clock synthesizer	Fixed to multiplication by eight, f_{XX} = 32 to 64 MHz	Fixed to multiplication by eight, f_{XX} = 32 to 64 MHz	Fixed to multiplication by eight, f_{XX} = 20 to 32 MHz	Fixed to multiplication by eight, f_{XX} = 20 MHz
PLL operation specifiable by PLLSIN pin	Yes	Yes	No	No

Remark f_{XX}: System clock frequency

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents related to V850E/IA3, V850E/IA4, V850ES/IK1, and V850ES/IE2

Document Name	Document No.
V850E1 Architecture User's Manual	U14559E
V850E/IA3, V850E/IA4 Hardware User's Manual	U16543E
V850ES Architecture User's Manual	U15943E
V850ES/IK1 Hardware User's Manual	U16910E
V850ES/IE2 Hardware User's Manual	U17716E
Inverter Control by V850 Series Vector Control by Hole Sensor Application Note	U17338E
Inverter Control by V850 Series Vector Control by Encoder Application Note	U17324E
Inverter Control by V850 Series 120° Excitation Method Control by Zero-Cross Detection Application Note	U17209E
Manual for Using Sample Program Functions Serial Communication (UARTA) (V850E/IA3, V850E/IA4, V850ES/IK1, V850ES/IE2) Application Note	U18233E
Manual for Using Sample Program Functions Serial Communication (CSIB) (V850E/IA3, V850E/IA4, V850ES/IK1, V850ES/IE2) Application Note	U18234E
Manual for Using Sample Program Functions DMA Functions (V850E/IA3, V850E/IA4) Application Note	U18235E
Manual for Using Sample Program Functions Timer M (V850E/IA3, V850E/IA4, V850ES/IK1, V850ES/IE2) Application Note	U18236E
Manual for Using Sample Program Functions Watchdog Timer (V850E/IA3, V850E/IA4, V850ES/IK1, V850ES/IE2) Application Note	U18237E
Manual for Using Sample Program Functions Timer P (V850E/IA3, V850E/IA4, V850ES/IK1, V850ES/IE2) Application Note	U18238E
Manual for Using Sample Program Functions Timer Q (V850E/IA3, V850E/IA4, V850ES/IK1, V850ES/IE2) Application Note	U18239E
Manual for Using Sample Program Functions Timer ENC (V850E/IA3, V850E/IA4) Application Note	U18240E
Manual for Using Sample Program Functions Port Functions (V850E/IA3, V850E/IA4, V850ES/IK1, V850ES/IE2) Application Note	U18241E
Manual for Using Sample Program Functions Clock Generator (V850E/IA3, V850E/IA4, V850ES/IK1, V850ES/IE2) Application Note	This manual
Manual for Using Sample Program Functions Standby Functions (V850E/IA3, V850E/IA4, V850ES/IK1, V850ES/IE2) Application Note	U18243E
Manual for Using Sample Program Functions Interrupt Functions (V850E/IA3, V850E/IA4, V850ES/IK1, V850ES/IE2) Application Note	U18244E
Manual for Using Sample Program Functions A/D Converters 0 and 1 (V850E/IA3, V850E/IA4, V850ES/IK1, V850ES/IE2) Application Note	U18245E
Manual for Using Sample Program Functions A/D Converter 2 (V850E/IA3, V850E/IA4) Application Note	U18246E

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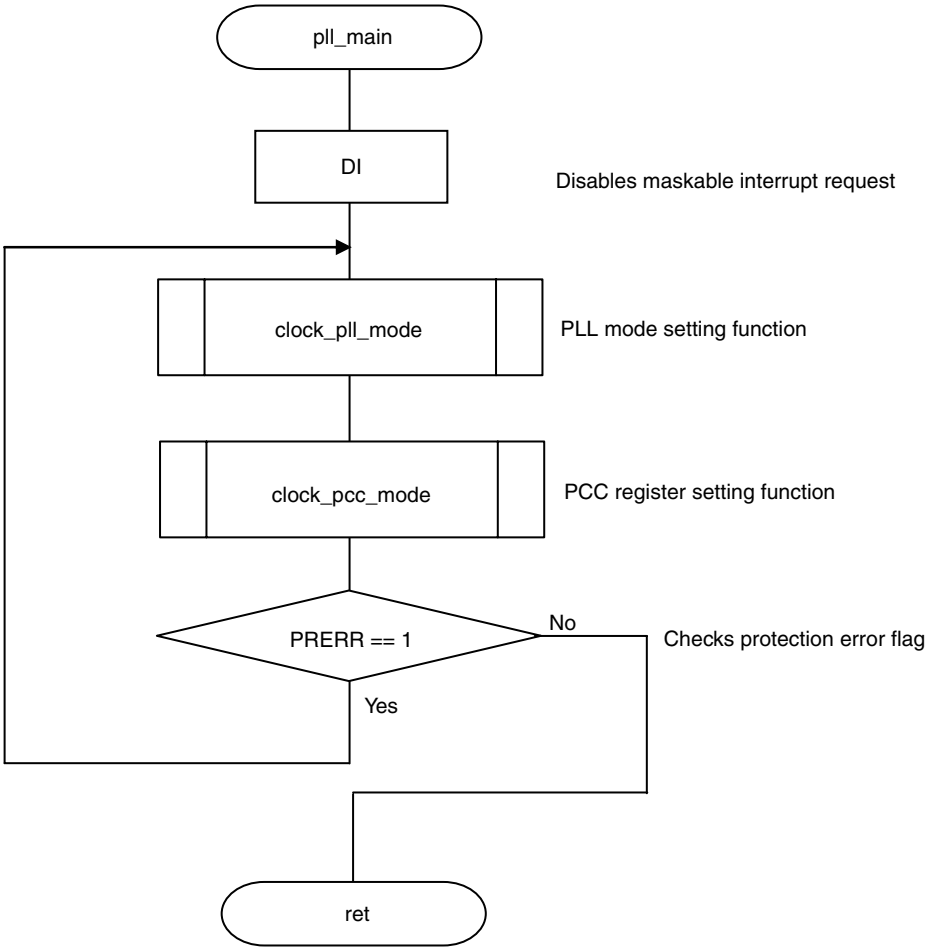
PLL mode

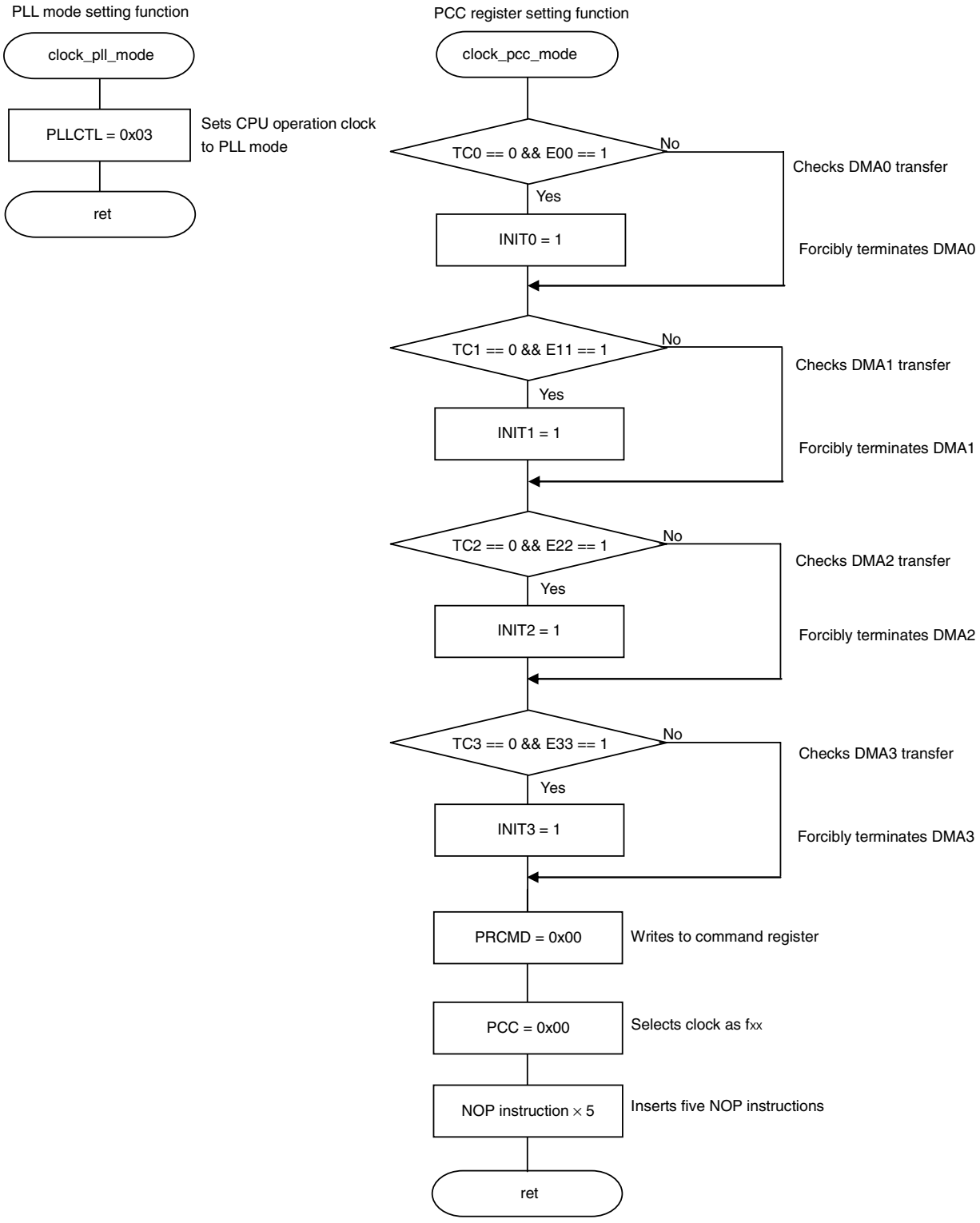
[Function]	Sets the clock frequency by setting the CPU operation clock (PLL mode) and the PCC register which is a special register.
[Function name]	pll_main
[Argument]	None
[Processing content]	Calls the PLL setting function by stopping all DMAs in use.
[Starting method]	None
[SFR used]	None
[call functions]	clock_pll_mode, clock_pcc_mode
[Variable]	None
[Interrupt]	None
[Interrupt source]	None
[File name]	clock_generator1.c
[Caution]	Note that if the pll_main function is called the maskable interrupt request will not be enabled (EI).

[Function name]	clock_pll_mode
[Processing content]	Sets to PLL mode by the PLLCTL register.
[SFR used]	PLLCTL: 0x03 (Sets to PLL mode.)
[call function]	None
[Variable]	None
[File name]	clock_generator1.c
[Caution]	None

[Function name]	clock_pcc_mode	
[Processing content]	Sets the PCC register by forcibly terminating DMA transfer.	
[SFRs used]	DCHC0.TC0	DMA0 transfer status bit
	DCHC0.E00:	1 (Enables DMA0 transfer.)
	DCHC0.INIT0:	1 (Forcibly terminates DMA0 transfer.)
	DCHC1.TC1	DMA1 transfer status bit
	DCHC1.E11:	1 (Enables DMA1 transfer.)
	DCHC1.INIT1:	1 (Forcibly terminates DMA1 transfer.)
	DCHC2.TC2	DMA2 transfer status bit
	DCHC2.E22:	1 (Enables DMA2 transfer.)
	DCHC2.INIT2:	1 (Forcibly terminates DMA2 transfer.)
	DCHC3.TC3	DMA3 transfer status bit
	DCHC3.E33:	1 (Enables DMA3 transfer.)
	DCHC3.INIT3:	1 (Forcibly terminates DMA3 transfer.)
	PRCMD:	0x00 (Writes to command register (used when writing to a special register).)
	PCC:	0x00 (Selects clock as f_{XX}.)
[call function]	None	
[Variable]	None	
[File name]	clock_generator1.c	
[Caution]	• DMA transfer is forcibly terminated in this sample program, because all DMA transfers must be terminated before performing data setting to the special register. • Set the PCC register after switching to the PLL mode. The PCC register is a special register and can therefore only be written in a combination of specific sequences.	

PLL mode (1/2)


pll_main
DI
Disables maskable interrupt request
clock_pll_mode
PLL mode setting function
clock_pcc_mode
PCC register setting function
PRERR == 1
No
Checks protection error flag
Yes
ret


PLL mode setting function
clock_pll_mode
PLLCTL = 0x03
Sets CPU operation clock to PLL mode
ret
PCC register setting function
clock_pcc_mode
TC0 == 0 && E00 == 1
No
Yes
Checks DMA0 transfer
INIT0 = 1
Forcibly terminates DMA0
TC1 == 0 && E11 == 1
No
Yes
Checks DMA1 transfer
INIT1 = 1
Forcibly terminates DMA1
TC2 == 0 && E22 == 1
No
Yes
Checks DMA2 transfer
INIT2 = 1
Forcibly terminates DMA2
TC3 == 0 && E33 == 1
No
Yes
Checks DMA3 transfer
INIT3 = 1
Forcibly terminates DMA3
PRCMD = 0x00
Writes to command register
PCC = 0x00
Selects clock as fxx
NOP instruction × 5
Inserts five NOP instructions
ret

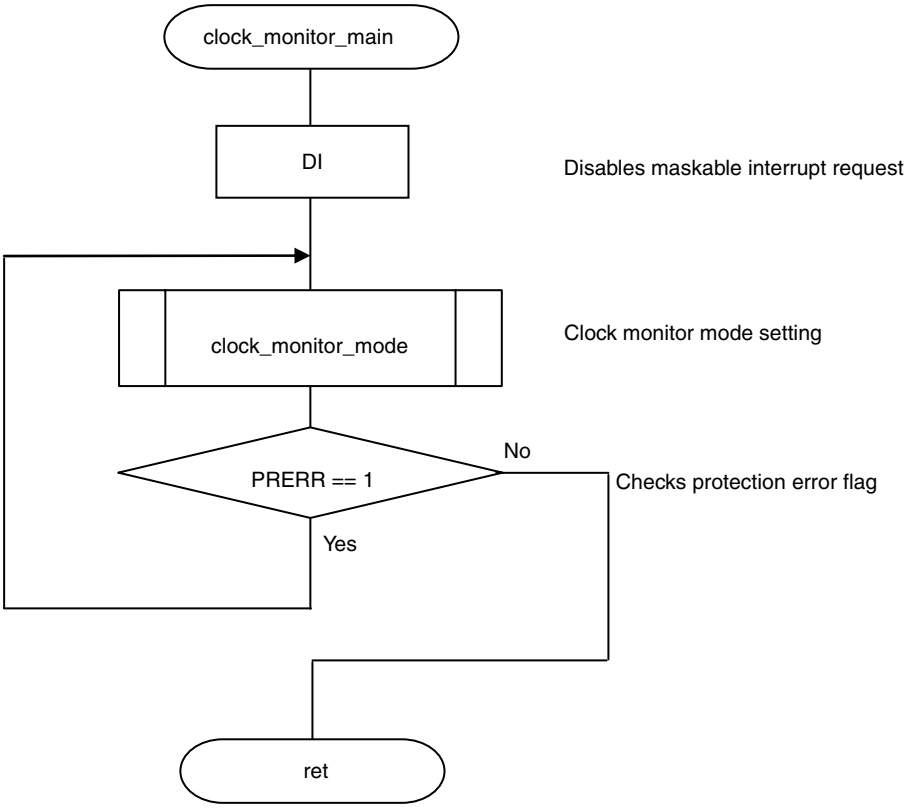
Clock generator

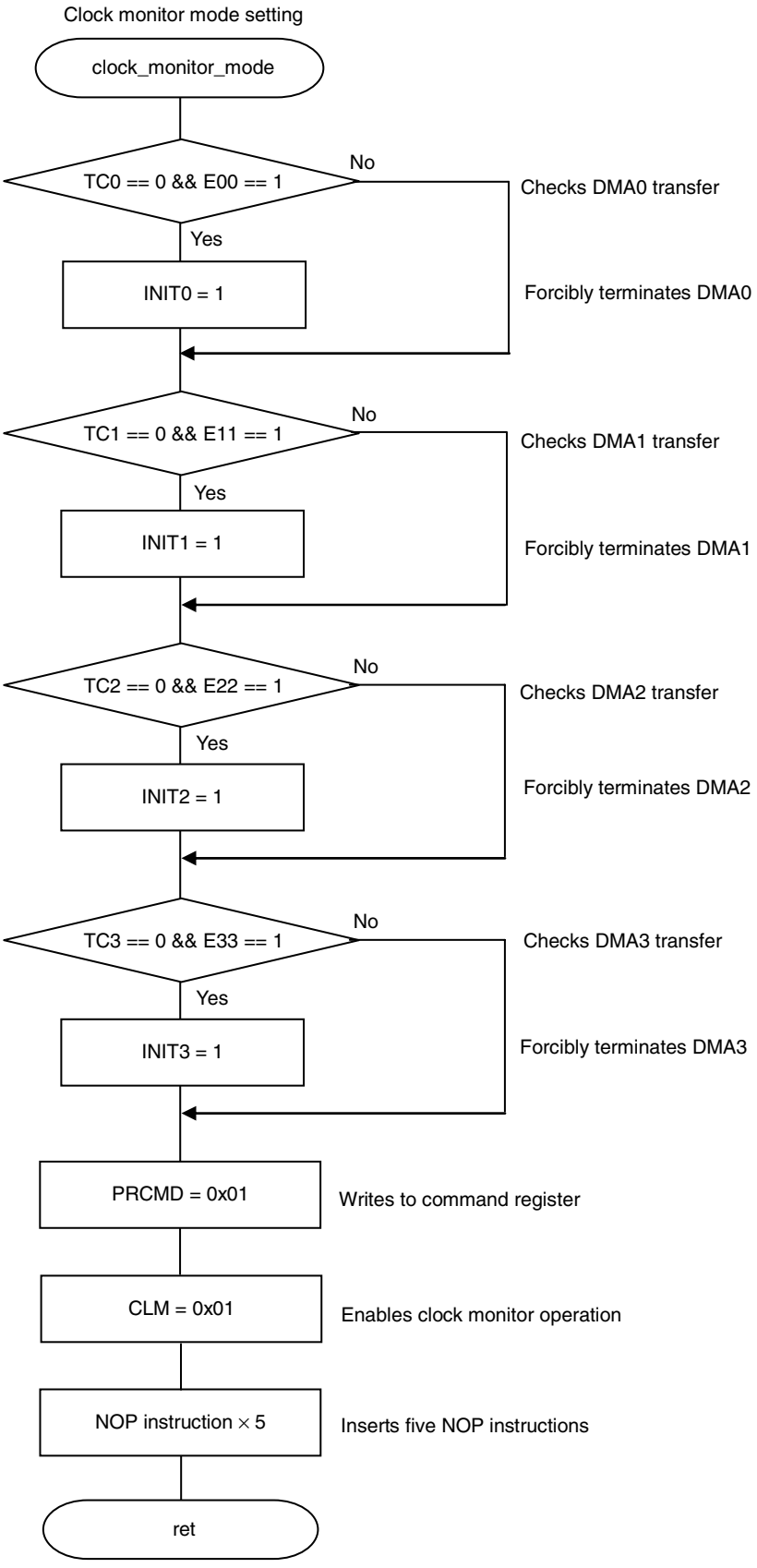
Clock monitor mode

[Function]	Performs clock monitor operation.
[Function name]	clock_monitor_main
[Argument]	None
[Processing content]	Enables operation of the clock monitor mode by calling the clock monitor mode function.
[Starting method]	None
[SFR used]	None
[call function]	clock_monitor_mode
[Variable]	None
[Interrupt]	None
[Interrupt source]	None
[File name]	clock_generator2.c
[Caution]	Note that if the clock_monitor_main function is called the maskable interrupt request will not be enabled (EI).

[Function name]	clock_monitor_mode	
[Processing content]	Sets the operation mode of the clock monitor via the CLM register, by forcibly terminating DMA transfer.	
[SFRs used]	DCHC0.TC0	DMA0 transfer status bit
	DCHC0.E00:	1 (Enables DMA0 transfer.)
	DCHC0.INIT0:	1 (Forcibly terminates DMA0 transfer.)
	DCHC1.TC1	DMA1 transfer status bit
	DCHC1.E11:	1 (Enables DMA1 transfer.)
	DCHC1.INIT1:	1 (Forcibly terminates DMA1 transfer.)
	DCHC2.TC2	DMA2 transfer status bit
	DCHC2.E22:	1 (Enables DMA2 transfer.)
	DCHC2.INIT2:	1 (Forcibly terminates DMA2 transfer.)
	DCHC3.TC3	DMA3 transfer status bit
	DCHC3.E33:	1 (Enables DMA3 transfer.)
	DCHC3.INIT3:	1 (Forcibly terminates DMA3 transfer.)
	PRCMD:	0x01 (Writes to command register (used when writing to a special register).)
	CLM:	0x01 (Sets to operation enable.)
[call function]	None	
[Variable]	None	
[File name]	clock_generator2.c	
[Cautions]	• DMA transfer is forcibly terminated in this sample program, because all DMA transfers must be terminated before performing data setting to the special register. • The CLM register is a special register and can therefore only be written in a combination of specific sequences.	

Clock monitor mode (1/2)




Clock monitor mode setting
clock_monitor_mode
TC0 == 0 && E00 == 1
No
Checks DMA0 transfer
Yes
INIT0 = 1
Forcibly terminates DMA0
TC1 == 0 && E11 == 1
No
Checks DMA1 transfer
Yes
INIT1 = 1
Forcibly terminates DMA1
TC2 == 0 && E22 == 1
No
Checks DMA2 transfer
Yes
INIT2 = 1
Forcibly terminates DMA2
TC3 == 0 && E33 == 1
No
Checks DMA3 transfer
Yes
INIT3 = 1
Forcibly terminates DMA3
PRCMD = 0x01
Writes to command register
CLM = 0x01
Enables clock monitor operation
NOP instruction × 5
Inserts five NOP instructions
ret

For further information, please contact:

NEC Electronics Corporation
1753, Shimonumabe, Nakahara-ku,
Kawasaki, Kanagawa 211-8668,
Japan
Tel: 044-435-5111
http://www.necel.com/

[America]

NEC Electronics America, Inc.
2880 Scott Blvd.
Santa Clara, CA 95050-2554, U.S.A.
Tel: 408-588-6000
800-366-9782
http://www.am.necel.com/

[Europe]

NEC Electronics (Europe) GmbH
Arcadiastrasse 10
40472 Düsseldorf, Germany
Tel: 0211-65030
http://www.eu.necel.com/

Hanover Office
Podbielskistrasse 166 B
30177 Hannover
Tel: 0 511 33 40 2-0

Munich Office
Werner-Eckert-Strasse 9
81829 München
Tel: 0 89 92 10 03-0

Stuttgart Office
Industriestrasse 3
70565 Stuttgart
Tel: 0 711 99 01 0-0

United Kingdom Branch
Cygnus House, Sunrise Parkway
Linford Wood, Milton Keynes
MK14 6NP, U.K.
Tel: 01908-691-133

Succursale Française
9, rue Paul Dautier, B.P. 52
78142 Velizy-Villacoublay Cédex
France
Tel: 01-3067-5800

Sucursal en España
Juan Esplandiu, 15
28007 Madrid, Spain
Tel: 091-504-2787

Tyskland Filial
Täby Centrum
Entrance S (7th floor)
18322 Täby, Sweden
Tel: 08 638 72 00

Filiale Italiana
Via Fabio Filzi, 25/A
20124 Milano, Italy
Tel: 02-667541

Branch The Netherlands
Steijgerweg 6
5616 HS Eindhoven
The Netherlands
Tel: 040 265 40 10

[Asia & Oceania]

NEC Electronics (China) Co., Ltd
7th Floor, Quantum Plaza, No. 27 ZhiChunLu Haidian
District, Beijing 100083, P.R.China
Tel: 010-8235-1155
http://www.cn.necel.com/

NEC Electronics Shanghai Ltd.
Room 2511-2512, Bank of China Tower,
200 Yincheng Road Central,
Pudong New Area, Shanghai P.R. China P.C:200120
Tel: 021-5888-5400
http://www.cn.necel.com/

NEC Electronics Hong Kong Ltd.
12/F., Cityplaza 4,
12 Taikoo Wan Road, Hong Kong
Tel: 2886-9318
http://www.hk.necel.com/

NEC Electronics Taiwan Ltd.
7F, No. 363 Fu Shing North Road
Taipei, Taiwan, R. O. C.
Tel: 02-8175-9600
http://www.tw.necel.com/

NEC Electronics Singapore Pte. Ltd.
238A Thomson Road,
#12-08 Novena Square,
Singapore 307684
Tel: 6253-8311
http://www.sg.necel.com/

NEC Electronics Korea Ltd.
11F., Samik Lavied'or Bldg., 720-2,
Yeoksam-Dong, Kangnam-Ku,
Seoul, 135-080, Korea
Tel: 02-558-3737
http://www.kr.necel.com/

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