

Volume 64 (Jan 31, 2007)

Breakthrough in Setting Optimum System LSI Chips' Design Margins for the 65-nanometer Node and Beyond

As semiconductor devices evolve toward faster speeds and smaller features, it becomes increasingly difficult to ensure design margins sufficient enough to meet device performance targets, and increasingly more important to set the best possible margins to derive the full potential of device performance (Figure 1).

Interconnect variations in particular are starting to have an increasingly dominant effect on timing performance as geometries shrink, and have thus emerged as a critical factor in the determination of device performance (Figure 2).

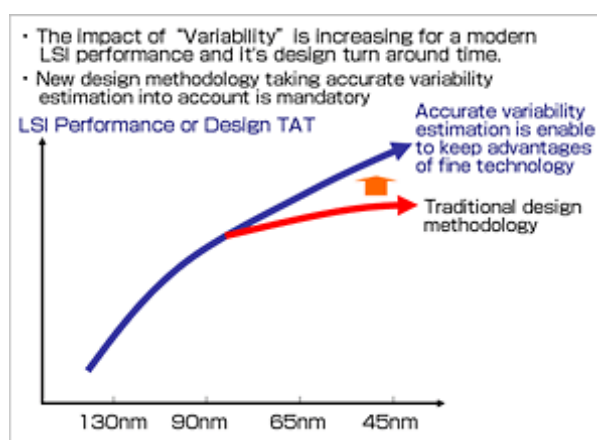


Figure 1 A Design Head Ache of Fine Technology

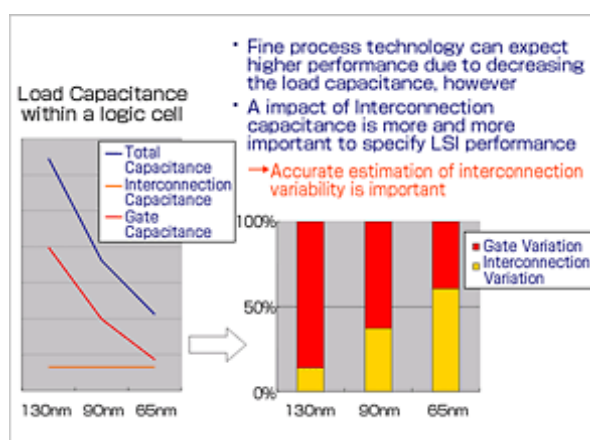


Figure 2 A Impact of Interconnection Variability

Interconnect variation is generally expressed in terms of parameters such as metal height, width, spacing, and so on, but to accommodate worst-case variations in these parameters, designers have used guardbanding and set margins larger than they need to be, which has prevented the full potential of a device's performance from being realized (Figure 3).

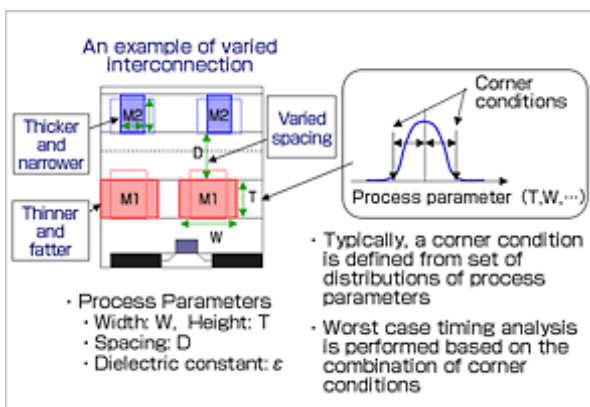


Figure 3 Interconnection variability and Corner conditions

NEC Electronics has achieved an R&D breakthrough toward solving this problem by developing and demonstrating a new design methodology that precisely models interconnect variation.

The key to this technique is the discovery that, for every type of wiring pattern, there is a constant ratio of variation between the individual parameters for wiring shape, namely width and thickness. This makes it possible to calculate statistically precise worst cases for total delay variation (Figure 4). Instead of simply combining the worst-case interconnect parameters, the worst-case total delay can be calculated by a statistical manner with considering statistically independent parameters.

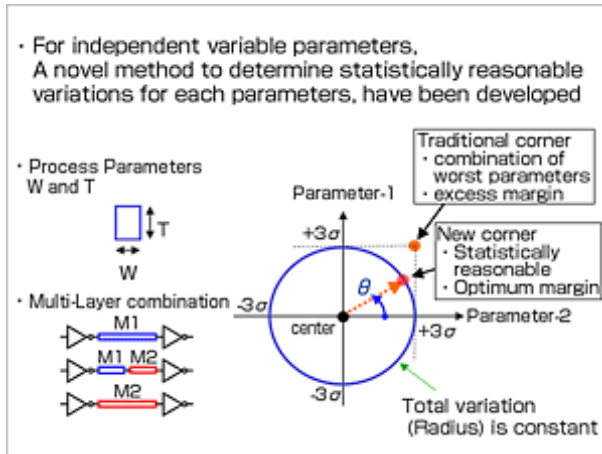


Figure 4 New Statistical Variable Aware Methodology

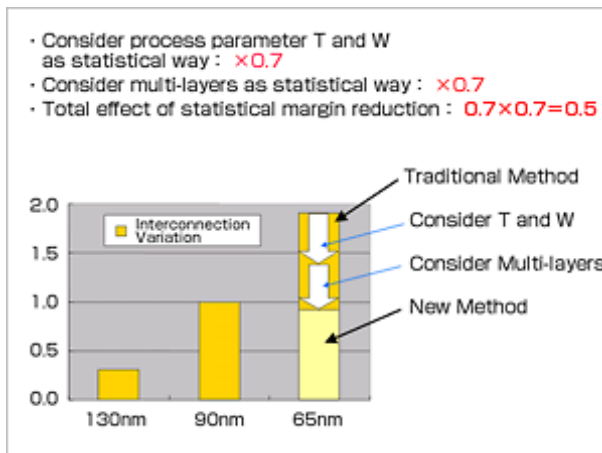


Figure 5 Effect of New Statistical Variable Aware Methodology

Compared to the conventional approach of simply combining worst-case conditions for each interconnect parameter, this new method enables us to significantly reduce the margin of interconnect capacitance (resistance) for the same interconnect wire within a single layer by 0.7 times (a 30% improvement). Furthermore, by factoring in the independence between interconnect parameters in multiple layers, we can reduce the interconnect capacitance by another 0.7 times (an additional 30% improvement). With this method, we are able to hold down the total variation to 0.7 to 0.5 times, thus enabling us to suppress interconnect delay variation for 65 nm processes to about the same level as we see currently for 90 nm processes (Figure 5).

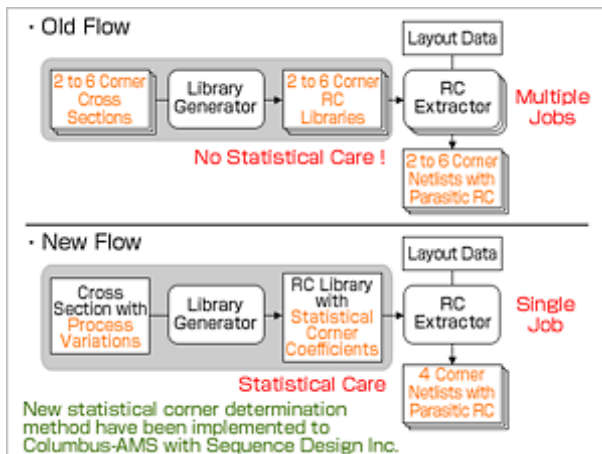


Figure 6 Design Flow

In collaboration with U.S.-based EDA tool vendor Sequence Design Inc., we incorporated our new method into Sequence's RC extraction design tool, Columbus-AMS. While offering the same flexibility and degree of freedom as other tools, Columbus-AMS extracts interconnect parameters with a very high degree of precision. Furthermore, the tool extracts an RC netlist for multiple worst-case corner conditions in a single iteration, to achieve markedly faster, more efficient design (Figure 6).

Ultimately NEC Electronics plans to implement a timing sign-off solution based on statistical timing analysis, but first we must develop a more viable and effective design technology based on the interconnect-variation, corner-model-generation technology developed in this work. Afterward we plan to move this technology out of the lab and into the marketplace as quickly as possible. NEC Electronics will continue its major R&D commitment to the rapid development and deployment of advanced statistical design solutions to meet the challenges of ever-smaller deep-submicron processes.

< Addendum >

The basic concept of the technology described here is outlined in a paper entitled "Statistical Corner Conditions of Interconnect Delay (Corner LPE Specifications)" presented at ASP-DAC 2006.

Terminology

Terminology	Explanation
RC extraction	A method for calculating the electrical characteristics of interconnects in LSI layouts based on resistance (R) and capacitance (C) components from the original drawn shapes. A type of electronic design automation (EDA) tool that performs these calculations.
Interconnect variation	Variations in width, height and other parameters of interconnecting metal lines on LSI chips caused by microfabrication equipment and processing conditions.
Delay variation	Divergence of on-chip circuit performance (speed, etc.) from target performance. Delay variations could be caused by a number of factors: variations in transistor parameters or variations in usage conditions—noise, temperature, voltage, and so on. Interconnect variation is one of the potential causes of delay variation.
Worst-case corner	Worst-case scenario when delay variation is at its worst. Parameter values of the parameters causing the variation can be combined.

Links

- 11th Asia and South Pacific Design Automation Conference ASP-DAC 2006
ASP-DAC 2006 Archives
 - 7C-1: Statistical Corner Conditions of Interconnect Delay (Corner LPE Specifications)

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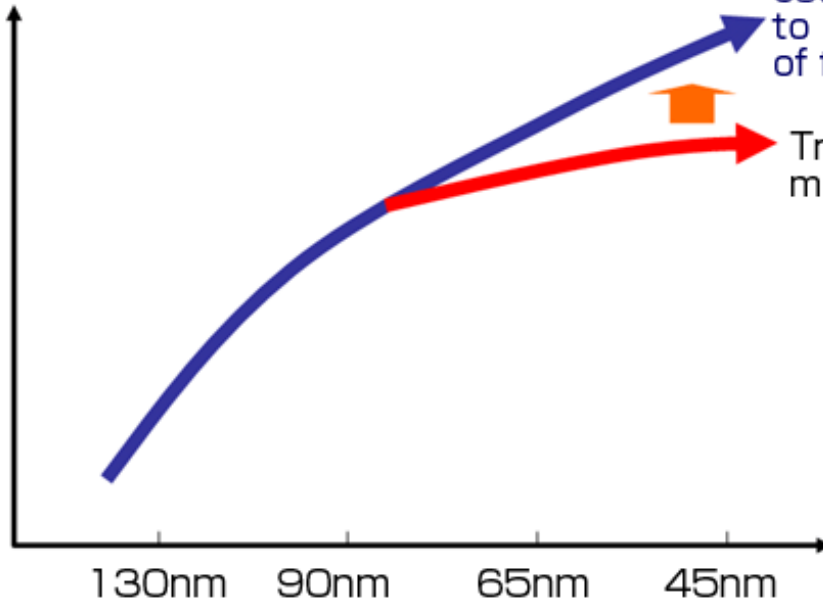
Was this article of interest to you?

Yes No

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- The impact of “Variability” is increasing for a modern LSI performance and it's design turn around time.
- New design methodology taking accurate variability estimation into account is mandatory

LSI Performance or Design TAT



Accurate variability estimation is enable to keep advantages of fine technology

Traditional design methodology

Figure 1 A Design Head Ache of Fine Technology

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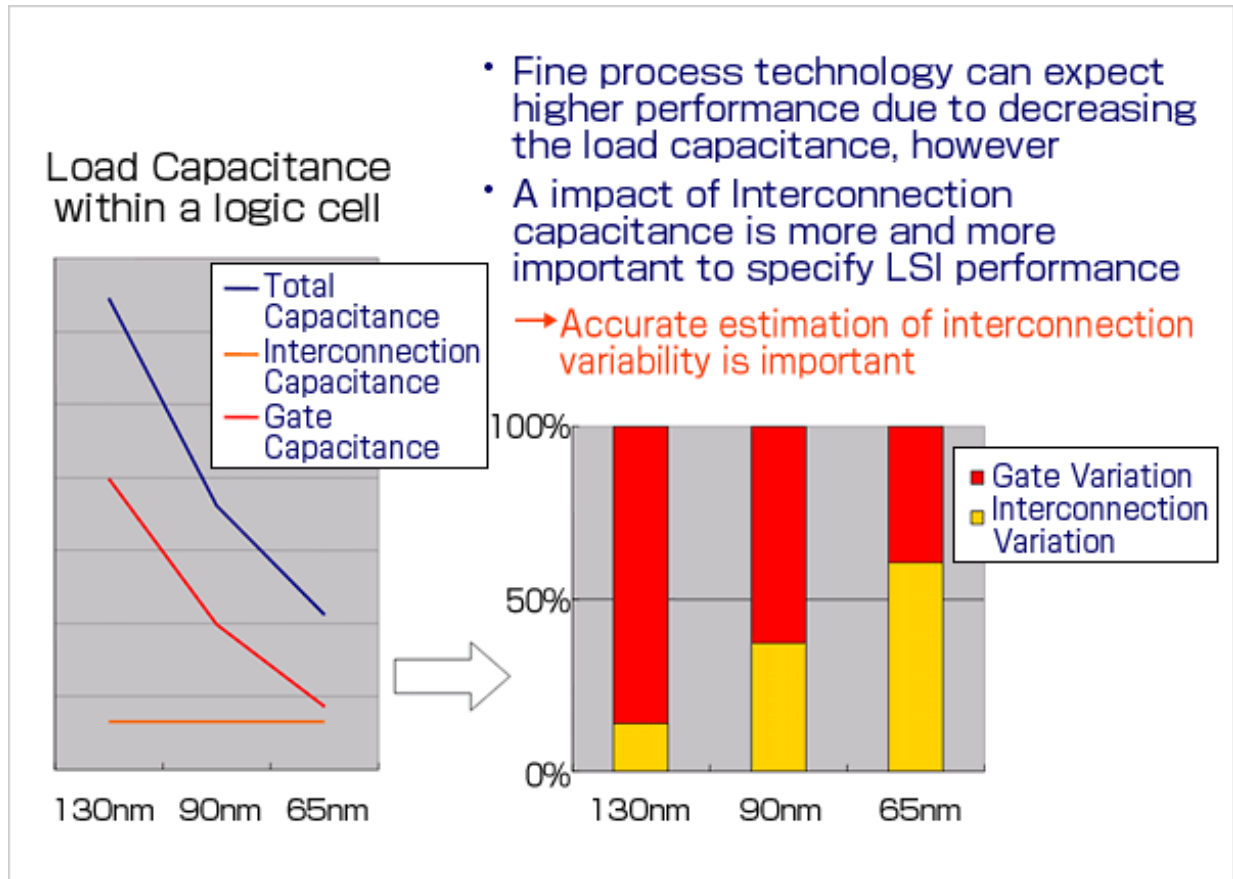


Figure 2 A Impact of Interconnection Variability

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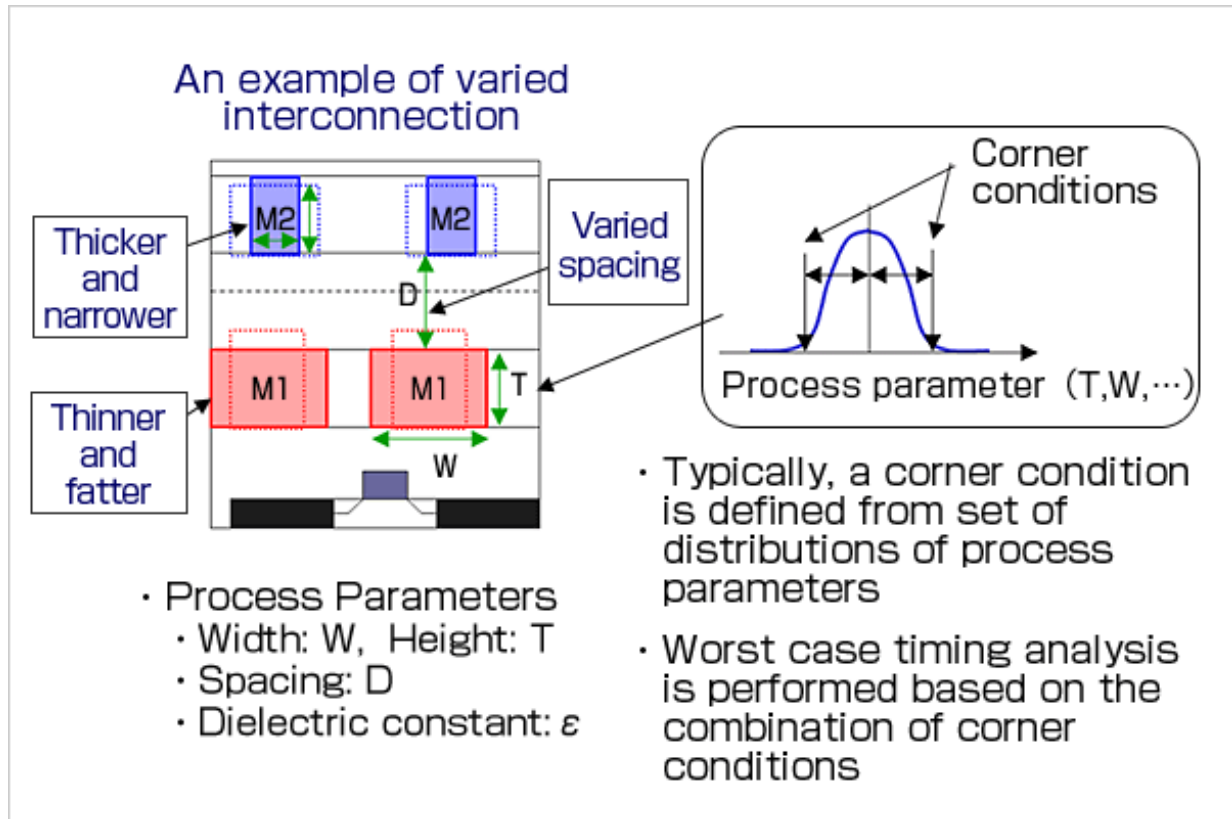


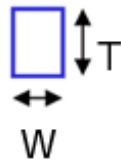
Figure 3 Interconnection variability and Corner conditions

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- For independent variable parameters, A novel method to determine statistically reasonable variations for each parameters, have been developed

- Process Parameters W and T



- Multi-Layer combination

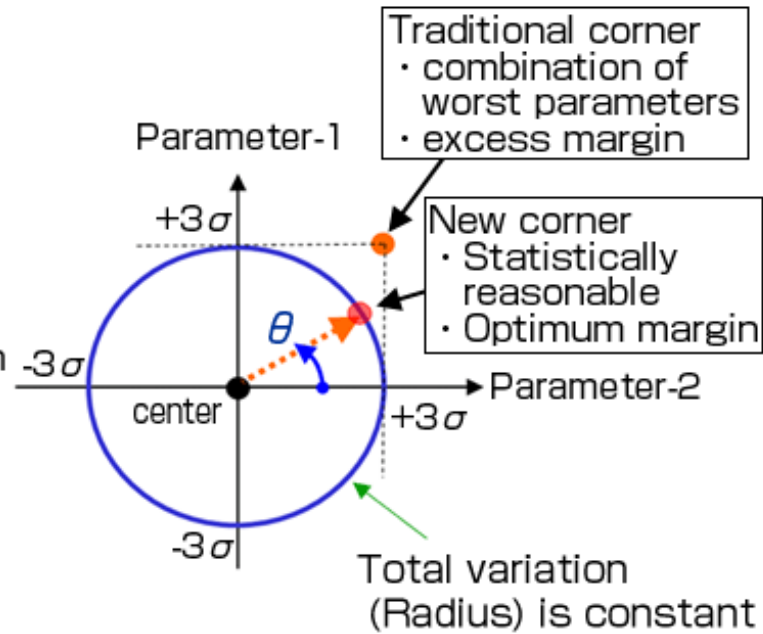
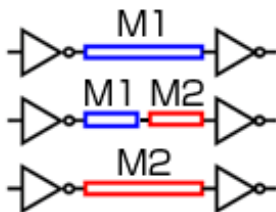


Figure 4 New Statistical Variable Aware Methodology

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- Consider process parameter T and W as statistical way : $\times 0.7$
- Consider multi-layers as statistical way : $\times 0.7$
- Total effect of statistical margin reduction : $0.7 \times 0.7 = 0.5$

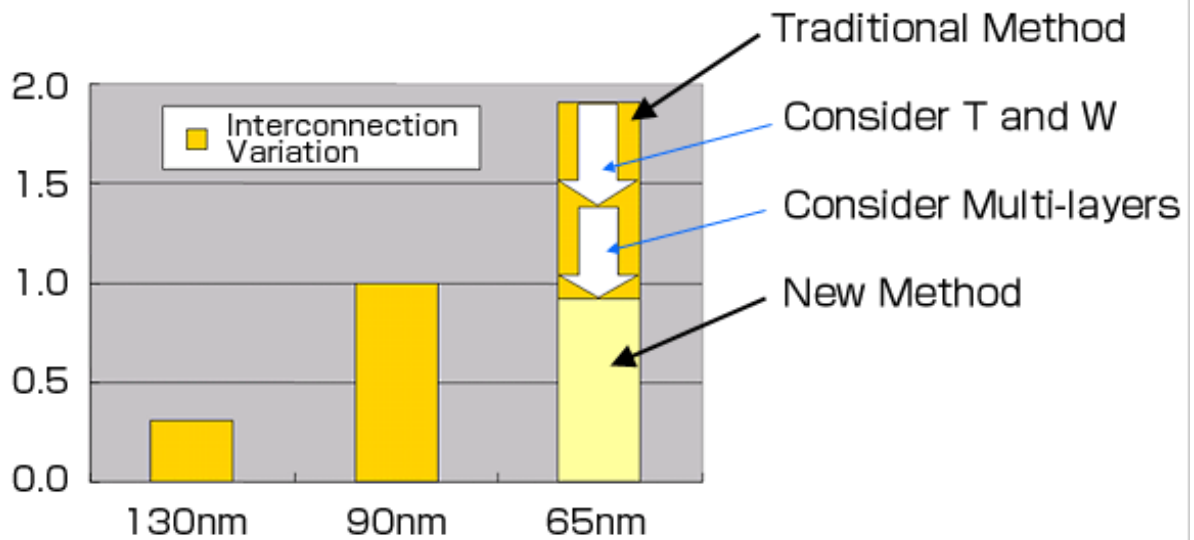


Figure 5 Effect of New Statistical Variable Aware Methodology

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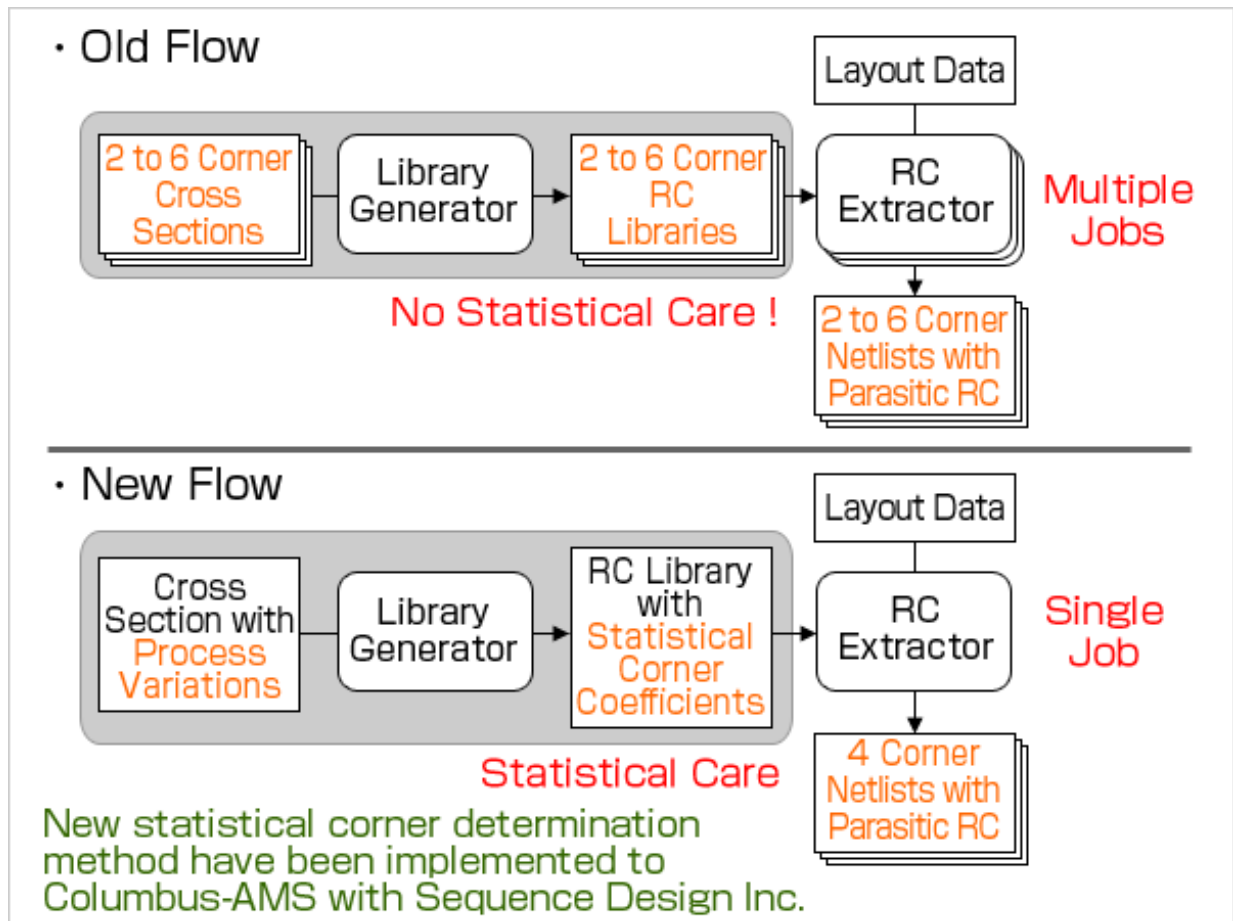


Figure 6 Design Flow

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