

**Information**

**NEC**

# **$\mu$ PD98408      Q&A**

**(NEASCOT-T20™)**

**6-PORT 25M ATM PHY LSI**

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## SUMMARY OF CONTENTS

CHAPTER 1 FUNCTIONS AND OPERATIONS .....	11
CHAPTER 2 ELECTRIC CHARACTERISTICS.....	15
CHAPTER 3 APPLICATION CIRCUITS.....	18
CHAPTER 4 OTHERS .....	23

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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## INTRODUCTION

- Target Readers** This manual is intended for engineers who wish to understand the functions of the  $\mu$ PD98408 and use it when designing application systems.
- Purpose** This manual aims to answer those questions frequently asked by users of this product and has been prepared as a reference for users if ever they need clarification of certain points.
- How to Read This Manual** Refer to the table of contents to locate the topic for which you require an explanation. Readers of this manual are required to have a basic understanding of electricity, logic circuits, and microcontrollers. When performing design, use the latest version of the user's manual (abbreviated to UM hereafter) and/or data sheet (abbreviated to DS hereafter).
- Related Documents**
- Data sheet: S12313E
  - User's manual: S11409E
- Conventions**
- |                     |  |
|---------------------|--|
| Data significance:  | Higher digits on the left, lower digits on the right       |
| Active low:         | XXX_B (_B following pin or signal name)                    |
| Memory map address: | Lower addresses on the top, higher addresses on the bottom |
| Numeric notation:   | Binary .....XXXX or XXXXB                                  |
|                     | Decimal.....XXXX   |
|                     | Hexadecimal.....XXXXh                                      |

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## CONTENTS

<b>CHAPTER 1 FUNCTIONS AND OPERATIONS</b> .....	<b>11</b>
<b>Q.1</b> The $\mu$ PD98408 has a six-port circuit UTP/STP interface. If only four of the ports are used, how should the pins of the unused ports be handled? .....	11
<b>Q.2</b> LOS occurs on power application. Is this normal? .....	11
<b>Q.3</b> Does the $\mu$ PD98408 output random data to the circuit even in idle status (when there is no command or valid transmit data to send)? .....	11
<b>Q.4</b> How long does it take the $\mu$ PD98408 to actually output the X_8 command to the circuit after a pulse signal is input to the SIN pin to transmit the X_8 command? .....	12
<b>Q.5</b> When is the X_X command transmitted to the circuit after power on (reset)?.....	12
<b>Q.6</b> Is the data transmitted to the circuit during-loop back execution and is the data converted into 4B5B? .....	13
<b>Q.7</b> Is it possible to specify whether a received idle/unassigned cell is discarded inside the $\mu$ PD98408?.....	13
<b>Q.8</b> How does the $\mu$ PD98408 operate if it receives a short cell of less than 53 bytes from the circuit?.....	13
<b>Q.9</b> Does the $\mu$ PD98408 automatically reset the FIFO to discard cells from the internal transmit/receive FIFO if the FIFO overflows? .....	14
<b>Q.10</b> The transmit FIFO has a depth of three cells. How many cells in this FIFO cause the $\mu$ PD98408 to start transmitting data to the circuit side?.....	14
<b>CHAPTER 2 ELECTRIC CHARACTERISTICS</b> .....	<b>15</b>
<b>Q.11</b> Can an ambient operating temperature ( $T_A$ ) range of $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ be supported? .....	15
<b>Q.12</b> Isn't the logic of the RW_B signal reversed in the timing chart of the CPU interface write operation (BUSMODE = 0) in Electric Characteristics of the second edition of the Data Sheet?.....	16
<b>Q.13</b> How long is the DATA determination time (vs. RD_B $\downarrow$ )? .....	17
<b>CHAPTER 3 APPLICATION CIRCUITS</b> .....	<b>18</b>
<b>Q.14</b> Can you recommend a transformer module that can be connected to the $\mu$ PD98408?.....	18
<b>Q.15</b> Could you provide a board layout example? .....	20
<b>CHAPTER 4 OTHERS</b> .....	<b>23</b>
<b>Q.16</b> Is the BSDL (Boundary Scan Description Language) file available? .....	23

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## CHAPTER 1 FUNCTIONS AND OPERATIONS

### Q.1

The  $\mu$ PD98408 has a six-port circuit UTP/STP interface. If only four of the ports are used, how should the pins of the unused ports be handled?

### A.1

Handle the unused port pins as follows:

- Receive pins (RDIP0 to 5, RDIN0 to 5) → Pull up via resistor (1 k $\Omega$ )
- Send pins (TDOP0 to 5, TDON0 to 5) → Leave open
- AV<sub>DD</sub> pin → Connect to the V<sub>DD</sub> plane of the board
- AGND pin → Connect to the GND plane of the board

Set the unused pins to standby mode (PMDSTB = 1) by using the PMD standby register (PMDSTBY).

**Reference:** 2.2 RECOMMENDED CONNECTION FOR UNUSED PINS, UM

### Q.2

LOS occurs on power application. Is this normal?

### A.2

Yes.

LOS occurs in all the circuits of the  $\mu$ PD98408 immediately after the power is applied (reset), and it takes at least 224  $\mu$ s to clear LOS. Read the LOS occurrence information register (LOSERR) after connecting the circuit and confirm that the  $\mu$ PD98408 has recovered from LOS (LSn bit = 0). Then, unmask the interrupt that has occurred as a result of LOS.

**Reference:** Note in 3.7.1 LOS (Loss of Signal) Detection Function, UM

### Q.3

Does the  $\mu$ PD98408 output random data to the circuit even in idle status (when there is no command or valid transmit data to send)?

### A.3

The  $\mu$ PD98408 outputs random data to the circuit, even in idle status.

This is because the  $\mu$ PD98408 is scrambled even in idle status and transmits dummy data, encoded into 4B5B blocks, to the other station. This dummy data prevents the other station from entering the LOS (Loss of Signal) status.

**Reference:** 3.1.3 Clock and Data Recovery, UM

**Q.4**

How long does it take the  $\mu$ PD98408 to actually output the X\_8 command to the circuit after a pulse signal is input to the SIN pin to transmit the X\_8 command?

**A.4**

The X\_8 command is output to the circuit about 24 or 34 clocks (32-MHz system clock: TCLOCK) after the pulse signal is input to the SIN pin.

**Reference:** 3.8 X\_8 COMMAND CODE TRANSMIT/RECEIVE FUNCTION, UM

**Q.5**

When is the X\_X command transmitted to the circuit after power on (reset)?

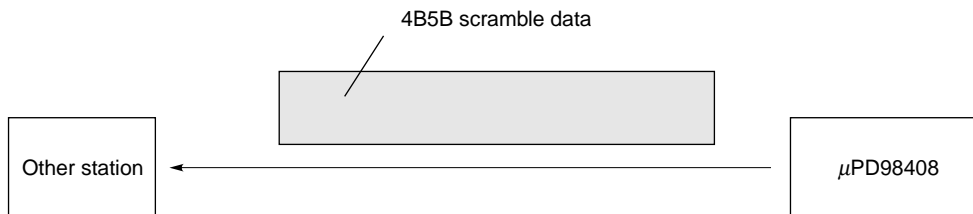
**A.5**

After power on (reset), the  $\mu$ PD98408 transmits the X\_X command to the other station at the beginning of the valid cell data that is transmitted first. (The X\_X command is inserted at the beginning of a valid cell to detect the boundary of the cell. It also directs resetting of the descrambler of the other station.) Prior to that point, the X\_X command is not transmitted.

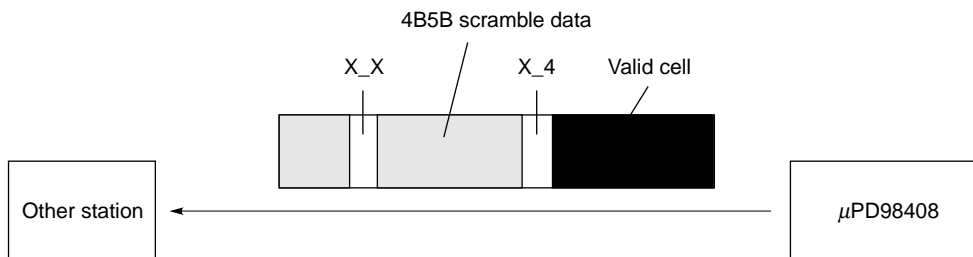
If the other station always detects a 4B5B code error, therefore, the descrambler of the other station is not reset after power on to the  $\mu$ PD98408 and before reception of the X\_X command that is prefixed to the first valid cell data. Consequently, a 4B5B code error (or symbol error) may occur.

The  $\mu$ PD98408 does not always detect a 4B5B code error. It detects only 4B5B code errors that occur in valid cell data, and ignores any 4B5B error that occurs in data other than the valid cell data. Even if the descrambler is not reset after power on (reset), therefore, a 4B5B code error does not occur.

**(1) After power on (reset) and before the transmission of the first valid cell**



**(2) When the first valid cell is transmitted**



**Reference:** 3.2.3 Command-Byte Insertion and Detection, UM

**Q.6**

Is the data transmitted to the circuit during-loop back execution and is the data converted into 4B5B?

**A.6**

The data transmitted to the circuit during the execution of PMD loop-back 1 and ATM layer loop-back can be selected by using the LBSEL1 and LBSEL0 bits of the command register (CMR). Whether 4B5B conversion is performed differs depending on this selection.

- Normal cell data (LBSEL1 = 0, LBSEL0 = 0): Transmits 4B5B-converted data.
- 010101... (LBSEL1 = 0, LBSEL0 = 1): Transmits non-4B5B-converted data.
- All 0 (LBSEL1 = 1, LBSEL0 = 0): Transmits non-4B5B-converted data.

**Reference:** 3.4 LOOP-BACK MODE, UM

**Q.7**

Is it possible to specify whether a received idle/unassigned cell is discarded inside the  $\mu$ PD98408?

**A.7**

Yes, it is possible.

Any of the following three modes can be selected by using the Idle cell discarding condition setting register (DMODE2).

Mode 1: Cells are discarded if VPI = 0 and GFC = PTC = LP = don't care.

Mode 2: Cells are discarded if VPI = VCI = GFC = 0 and PTC = LP = don't care.

Mode 3: Idle/unassigned cells are not discarded.

**Reference:** 3.2.7 Idle/Unassigned Cell Detection, UM

**Q.8**

How does the  $\mu$ PD98408 operate if it receives a short cell of less than 53 bytes from the circuit?

**A.8**

The discard cell counter register (DCCOU) does not count up.

The received short cell is discarded within the  $\mu$ PD98408 and is not output to the UTOPIA interface.

**Reference:** 4.2.5 Discarded Cell Counter (DCCOU: Default 00H), UM

**Q.9**

Does the  $\mu$ PD98408 automatically reset the FIFO to discard cells from the internal transmit/receive FIFO if the FIFO overflows?

**A.9**

The  $\mu$ PD98408 does not automatically reset the FIFO.

To forcibly discard the cells from the transmit/receive FIFO, it is necessary to reset the LSI. The cells cannot be forcibly discarded by disabling addresses with the ENn bit of the PHY address register (PHYADD).

Unless the LSI is reset, a garbage cell remaining in the transmit/receive FIFO is output to the external device.

**Reference:** 3.7.3 Transmit FIFO/Receive FIFO Overflow Detection Function and  
4.2.11 FIFO Overflow Registers (FIFOOVT/FIFOOVR: Default 00H), UM

**Q.10**

The transmit FIFO has a depth of three cells. How many cells in this FIFO cause the  $\mu$ PD98408 to start transmitting data to the circuit side?

**A.10**

One cell.

The  $\mu$ PD98408 starts transmitting data to the circuit side after it has completely read one cell from the UTOPIA interface.

**Reference:** 3.3.3 FIFO Block, UM

## CHAPTER 2 ELECTRIC CHARACTERISTICS

### Q.11

Can an ambient operating temperature ( $T_A$ ) range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  be supported?

### A.11

Yes.

The ambient operating temperature range of the  $\mu\text{PD98408}$ 's recommended operating conditions is  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

**Reference:** Recommended Operating Conditions in 2. ELECTRIC CHARACTERISTICS, DS

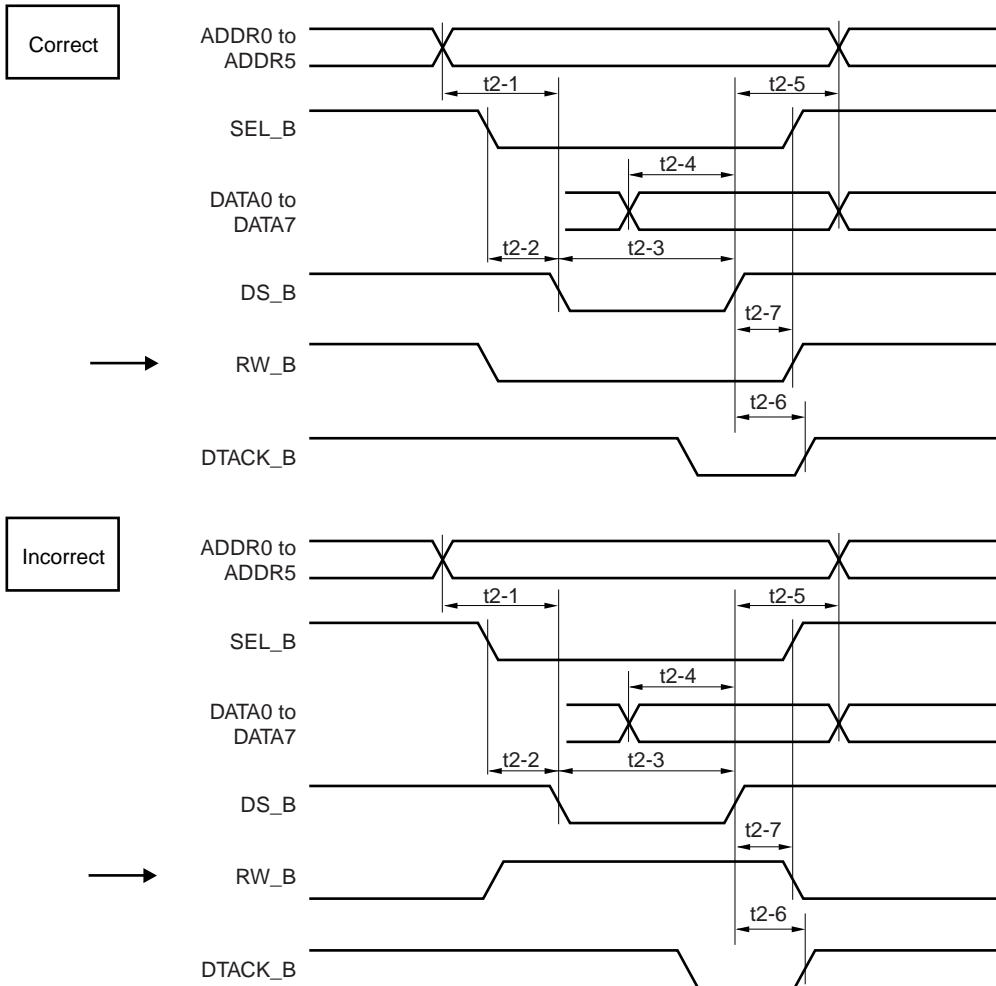
**Q.12**

Isn't the logic of the RW\_B signal reversed in the timing chart of the CPU interface write operation (BUSMODE = 0) in Electric Characteristics of the second edition of the Data Sheet?

**A.12**

Yes, the logic is reversed.

**CPU interface write operation (BUSMODE = 0)**



Reference: (3) Write operation (when BUSMODE = 0) in CPU Interface in 2. ELECTRIC CHARACTERISTICS, DS

**Q.13**

How long is the DATA determination time (vs. RD\_B↓)?

**A.13**

The DATA determination time (vs. RD\_B↓) is 42 ns MAX. (TCLOCK = 32 MHz).

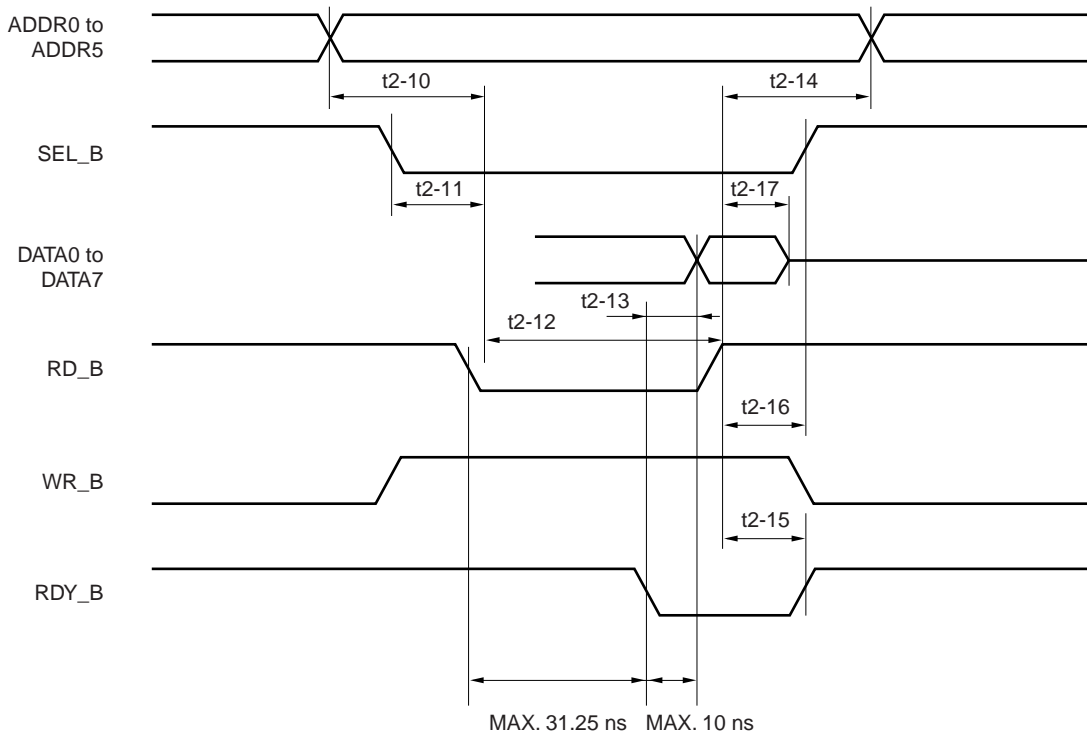
However, this value cannot be guaranteed because it is calculated, rather than actually measured.

The maximum value from RD\_B↓ to RDY\_B↓ is 31.25 ns that is equal to one cycle of TCLOCK.

The time required for data to be determined after RDY\_B↓ is 10 ns MAX., according to Electric Characteristics of the Data Sheet.

Therefore, the DATA determination time (vs. RD\_B↓) can be calculated as 31.25 + 10 = 41.25 ns.

**CPU Interface Read Operation (BUSMODE = 1)**



Reference: (2) Read operation (when BUSMODE = 1) in CPU Interface in 2. ELECTRIC CHARACTERISTICS, DS

## CHAPTER 3 APPLICATION CIRCUITS

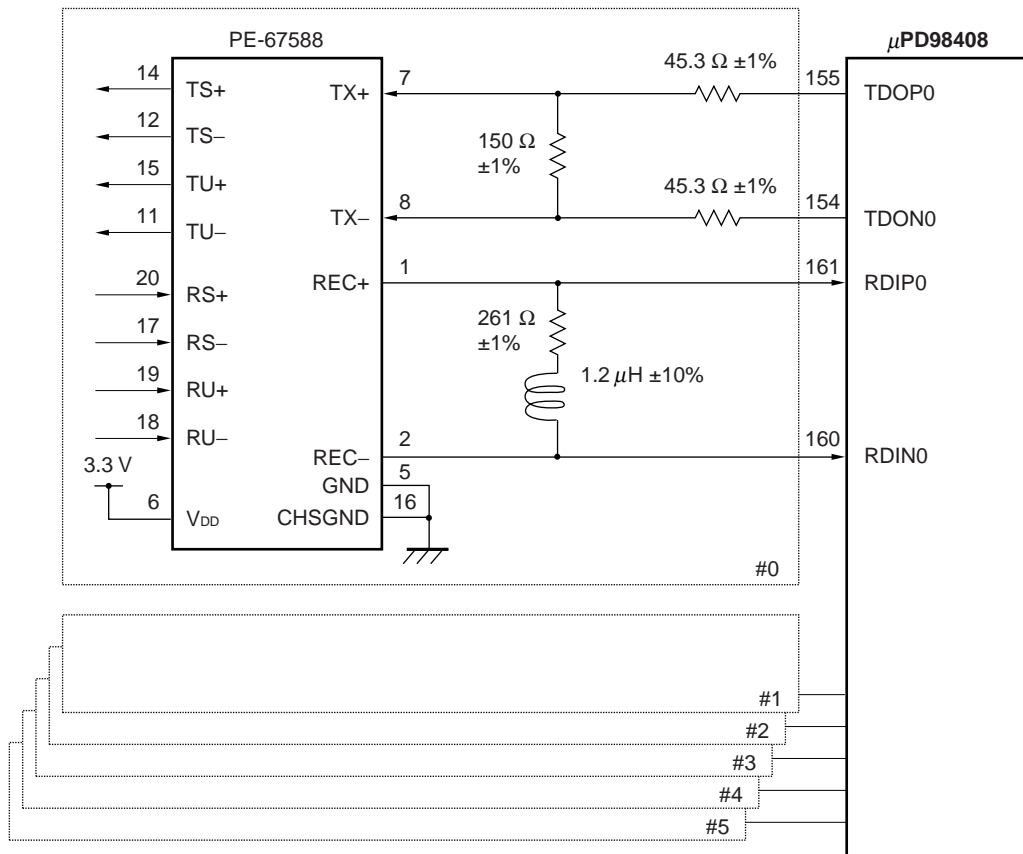
**Q.14**

Can you recommend a transformer module that can be connected to the  $\mu$ PD98408?

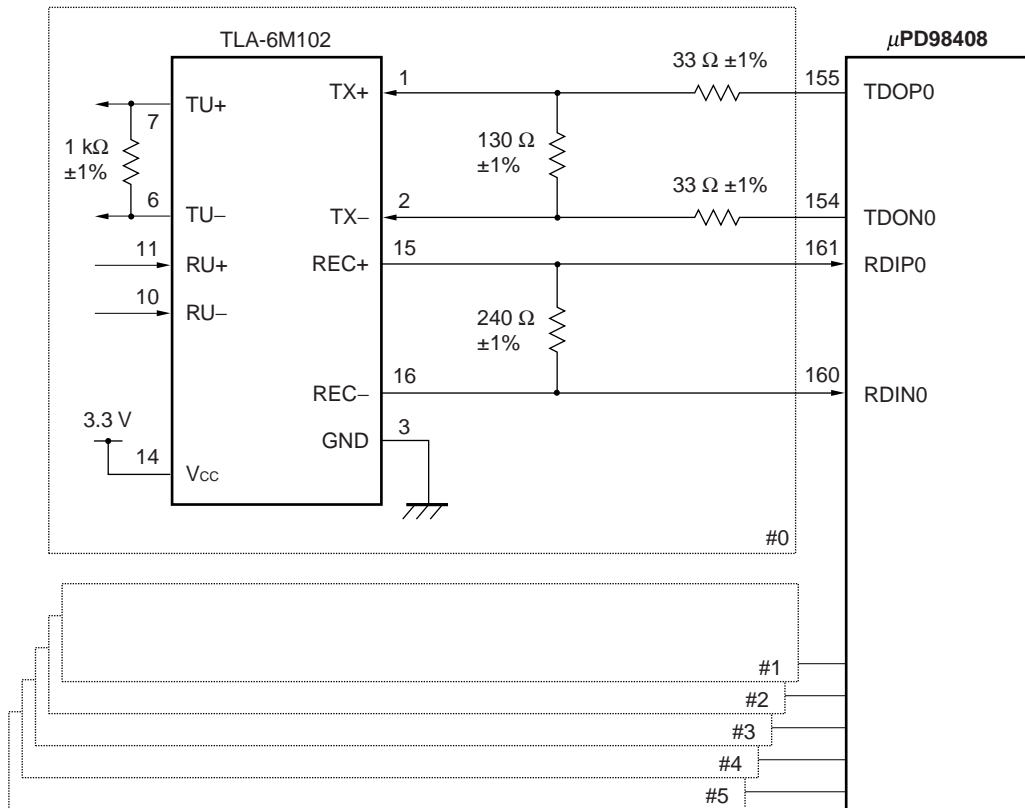
**A.14**

Two modules are recommended: the Pulse PE-67588 and the TDK TLA-6M102. Examples these units connection are shown below.

### 1. Example of connecting PE-67588



2. Example of connecting TLA-6M102



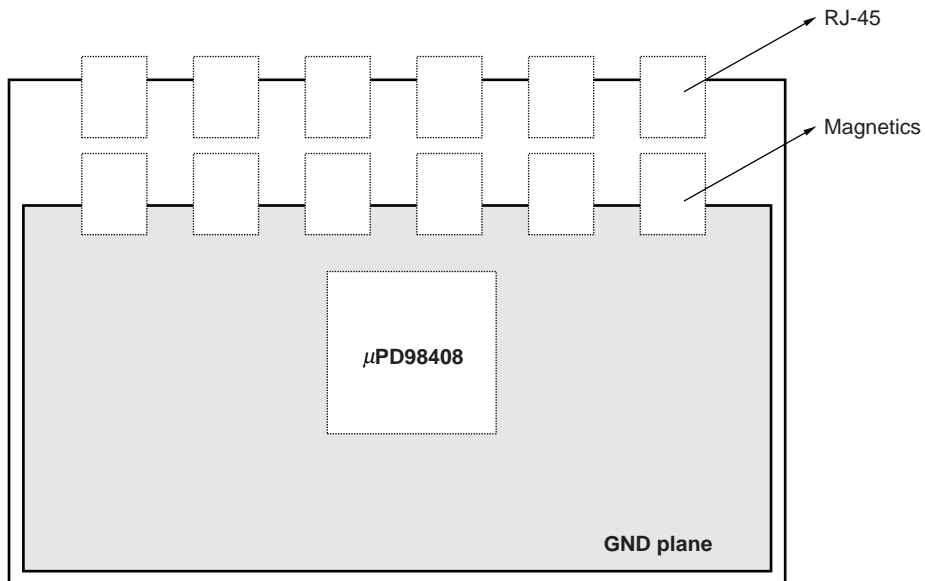
Reference: CHAPTER 6 THE EXAMPLE OF APPLICATION, UM

**Q.15**

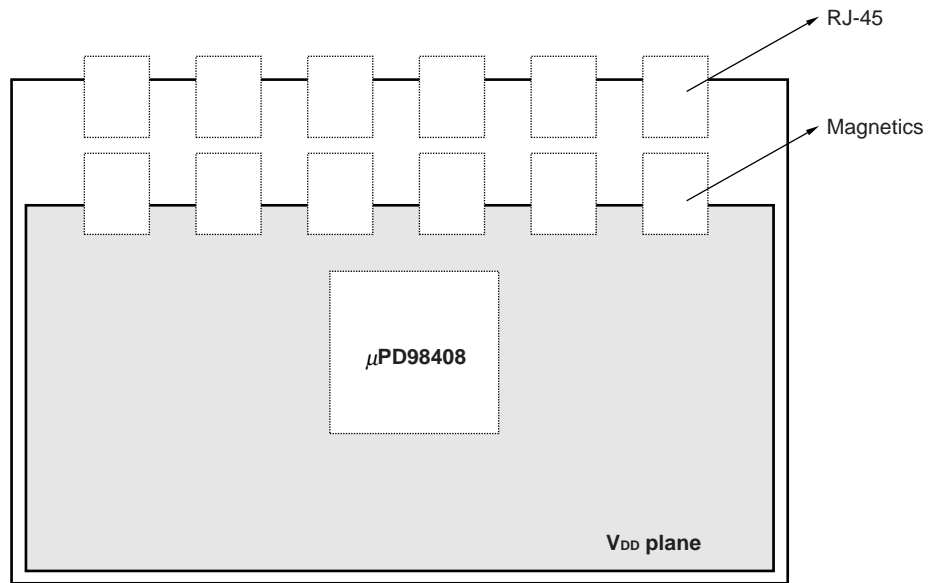
Could you provide a board layout example?

**A.15**

As follows:

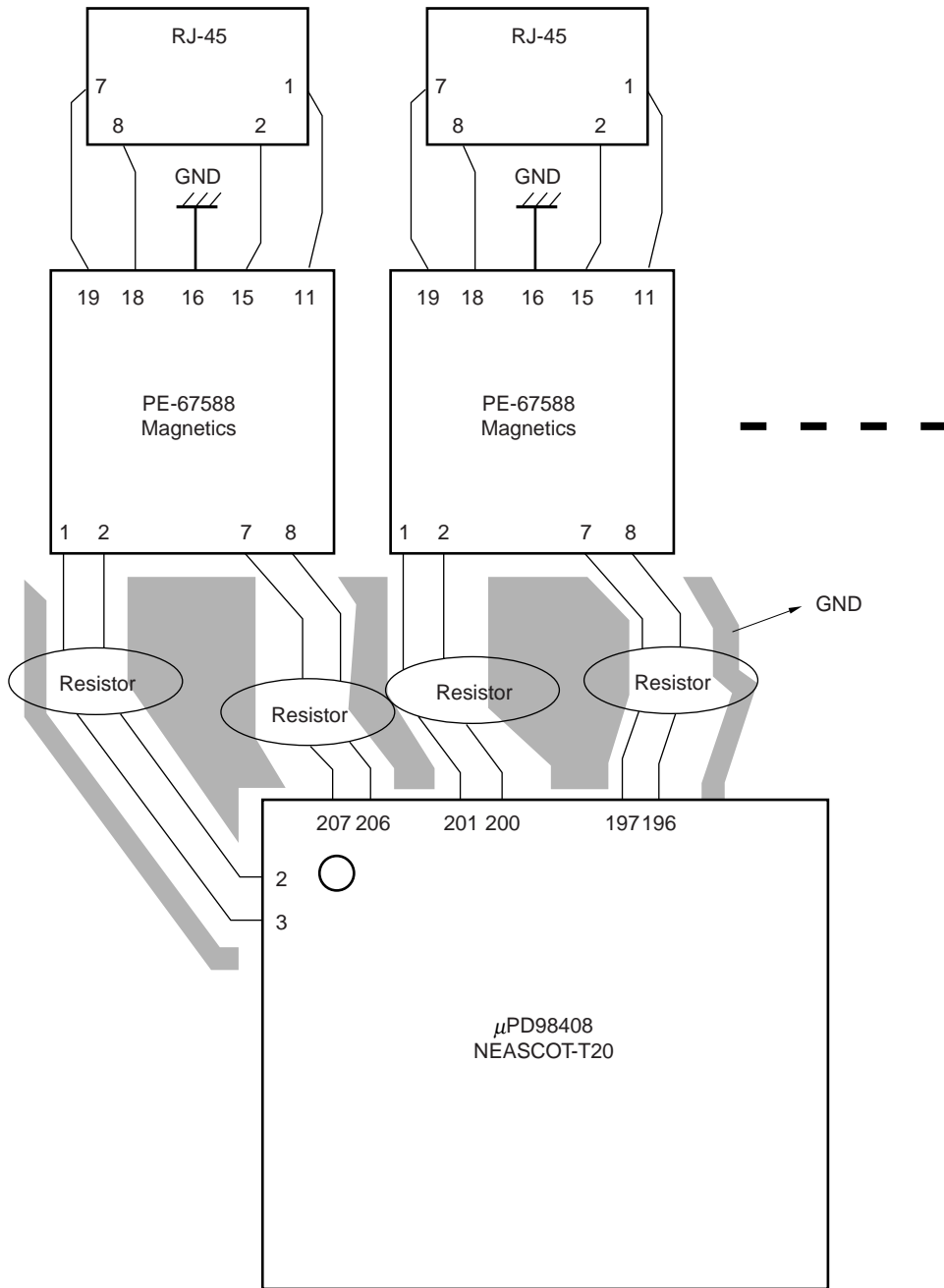
**(1) Ground (GND) plane**

- Remarks**
1. Connect AGND and DGND to the common plane. This plane should be as wide as possible.
  2. Do not locate the GND plane on half the area of the RJ-45 connector and the connector of the Magnetics.

**(2) Power ( $V_{DD}$ ) plane**

- Remarks**
1. Connect  $AV_{DD}$  and  $DV_{DD}$  to the common plane. This plane should be as wide as possible.
  2. Do not locate the  $V_{DD}$  plane on half the area of the RJ-45 connector or the connector of the Magnetics.

(3) Circuit side layout (with UTP cable and PE-67588)



- Remarks**
1. Keep the wiring between the RJ-45 connector and the Magnetics as short as possible.
  2. Keep the wiring between the Magnetics and the  $\mu$ PD98408 as short as possible.
  3. Use lines that are as strong and thick as possible as the GND and  $V_{DD}$  lines of the Magnetics.
  4. The signals between the Magnetics and the  $\mu$ PD98408 are very sensitive and susceptible to the signal lines nearby. It is therefore recommended that one pair of signal lines be separated from the other pair of signal lines by a GND pattern.

**Reference:** 6.3 BOARD LAYOUT, UM

## CHAPTER 4 OTHERS

### Q.16

Is the BSDL (Boundary Scan Description Language) file available?

### A.16

Yes, it is.

The BSDL file of the  $\mu$ PD98408 is available on request. For details, contact the NEC Semiconductor Technical Hotline, given at the end of this document.

**Reference:** CHAPTER 5 JTAG BOUNDARY SCAN, UM

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